NIPPON STEEL TECHNICAL REPORT No. 84 JULY 2001

UDC 621 . 3 . 049 . 77 : 661 . 665

# Large High-Quality Silicon Carbide Single Crystal Substrates

Noboru OHTANI*[1]
Tatsuo FUJIMOTO*[1]
Takashi AIGO*[1]
Masakazu KATSUNO*[1]
Hiroshi TSUGE*[2]
Hirokatsu YASHIRO*[1]

## Abstract

***This paper reviews the recent development of silicon carbide (SiC) single crystal substrates, focusing on Nippon Steel's development results. The potential of SiC semiconductors for high power, high frequency electronic devices and for use in severe environments has been recognized for several decades. Although such applications have long been hindered due to difficulty of its single crystal growth, large and high quality SiC single crystals have been brought into reality thanks to drastic improvements in the single crystal growth technology over the last few years. Using the developed single crystal substrates, high quality epitaxial layer growth and test manufacture of high performance devices are being energetically promoted. This paper introduces the current status of the SiC single crystal growth technology and discusses future challenges related to the technology.***

## 1. Introduction

The electronic industry has so far developed mostly on the basis of the electronic devices of Si single crystal materials. The Si single crystal will undoubtedly continue to be the main stay of the electronic industry because of its superiority over other semiconductor materials in any of the aspects of performance, costs or mass-productivity. It has recently been recognized, however, that the Si single crystal cannot be used in certain applications because of limits with regard to its material properties. In many technical fields, such as the aircraft and the automobile industries, for example, the use of electronic devices in high temperatures is sought after, but Si single crystals cannot be used in temperatures above 150°C.

More and more semiconductor devices are used in the field of electric power supply for AC-DC conversion and frequency conversion, etc. In this relation, higher control current and voltage, high speed operation and enhanced efficiency are required of the semiconductor devices, and for this reason, the limits in the material properties of the Si single crystal are being discussed. Silicon carbide (SiC) single crystal has attracted attention with the above background and also as a new electronic material to open a new field of technology.

Compared with the conventional Si devices, SiC devices offer five to ten times larger blocking voltages, several hundreds of degrees higher operating temperature and less than one-tenth of power losses. The SiC single crystal is attracting attention also as a substrate material for gallium nitride (GaN) semiconductor thin films, the applications of which to high-efficiency short wave-length optoelectronic devices and high-power mobile communication devices are presently in progress. Sapphire substrates have been mainly used for growing the GaN thin films, but SiC is more suitable for that purpose for the following reasons: far smaller difference of lattice constant and thermal expansion coefficient with GaN than sapphire; electric conductivity; higher thermal conductivity than sapphire; and it is cleavable.

Technologies to grow a thin epitaxial film on a SiC single crystal substrate, those of device design and device processes, indispensable for fabricating high performance devices of SiC, have lately shown rapid advances. Meanwhile, however, many aspects of the manufacturing technologies of the SiC single crystal substrates, which form a basis of the above technologies, are still left for future develop-

---

*[1] Technical Development Bureau

*[2] Personal & Labor Relations Div., presently studing in the USA

ments. In this sense, development of large diameter, high quality SiC single crystal is one of the key technologies in this field.

This report outlines the growth of SiC single crystals and describes characteristics of the SiC single crystals presently obtained, focusing on the authors recent research results.

## 2. Large Diameter SiC Single Crystal Growth

Excellent physical and electrical properties of the SiC single crystal have long been known. In view of its superior breakdown electric field, saturation electron drift velocity and thermal conductivity over the Si single crystal, research on the use of SiC for power devices and in severe environments were energetically pursued in the United States and Europe during the 1960s and 70s. That research using the SiC single crystals grown by the Acheson method or the Lely method yielded various reports suggesting high potential of SiC devices. The efforts were, however, discontinued at many institutes and laboratories as it became clear that the maximum crystal size achievable by the crystal growing methods could not surpass 10 to 15 mm. In 1978, amidst such thinking, Tairov and Tsvetkov of the former USSR proposed a modified Lely method to employ a seed crystal and atmosphere control[1)], wherein the control of the processes of crystal nucleation and material transfer was remarkably improved by introducing the seed crystal and atmosphere control using inert gas.

**Fig. 1** is a schematic illustration of the modified-Lely method using induction heating. The fundamental process of the method is that vapor of Si and C sublimated from a raw material in powder is transported by diffusion in an inert gas atmosphere in a semi-closed vessel and condenses in supersaturation onto the seed crystal kept at a lower temperature than the raw material. The growth rate of the crystal is, therefore, determined by the material temperature, and the temperature gradient and pressure in the vessel. The vessel, which is a graphite crucible placed in an inert gas (Ar) atmosphere, is heated by radio frequency induction. The temperature gradient is created by positioning the crucible asymmetrically to the induction coil center. The temperature control of the system is done generally by measuring the temperature of the crucible surface with an optical pyrometer through a hole in a heat insulation wall. The reading thus obtained is usually 2,200 to 2,400°C, but simulations and other estimation methods indicate that actual temperature inside the system is 2,500°C or higher. This very high process temperature is a distinguishing feature of the method while at the same time, it is the reason for the difficulty in controlling the crystal growing process and occurrence of defects.

The crystals Tairov et al obtained at first had a diameter as small as 18 mm, but the method has been brought up to be capable of producing crystals as large as 4 inches in diameter[2)]. The main diameter of the crystals now available in the market is 2 inches, with 3-inch diameter crystals having become available recently, though they have a limited specification. Considering the fact that production of 4-inch diameter wafers has been regarded as a milestone in the power device field for a long time, the modified-Lely method's capability to produce single crystals up to a diameter of 4 inches by a vapor phase crystal growth method deserves a special notice. Generally speaking, however, crystal quality tends to fall as the diameter becomes larger, and the above-mentioned large size crystals are no exception.

Absence of an established methodology is presumably the reason why it took so long to increase the size of the SiC single crystal. Difficulty in growing high quality single crystals increases rapidly as the diameter increases. Furthermore, various technical problems have become apparent during the course of diameter enlargement. Crystal growth temperature and the degree of supersaturation are largely different between the vapor phase crystal growth and the liquid phase crystal growth such as Si and gallium arsenide (GaAs), and this fact has hindered application of the long-accumulated technologies of the liquid phase semiconductor crystal growth to the manufacture of the SiC crystal. Over the last few years, however, simulation[3)] and other process optimization technologies have come to be applied to the SiC single crystal growth. Significance of simulation technologies is expected to increase in the crystal growth of this material system, in which in-situ monitoring is extremely difficult.

After a long period of concentrated efforts to achieve larger diameter SiC single crystals, Nippon Steel entered into a stage of rapid size increase thanks to the application of simulation and other related technologies. The SiC single crystal growth involves a material transportation process in a high temperature environment exceeding 2,500°C, where only a slight modification of a hot zone structure is known to exert a drastic influence over the crystal growth[4)]. For this reason, in reproducing the crystal growth in a simulator, it is necessary to deal with heat flow, material flow and chemical reactions in an integrated manner, but no such crystal growth simulator has been worked out yet. Nevertheless, Nippon Steel has succeeded in predicting crystal growth to some extent by systematically com-

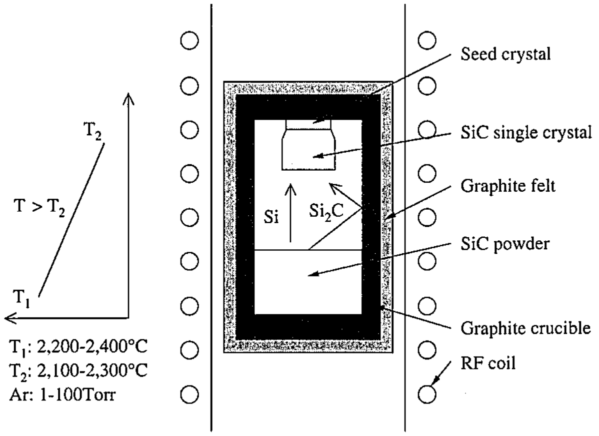


**Fig. 1 Schematic diagram of sublimation growth method (Modified-Lely method)**

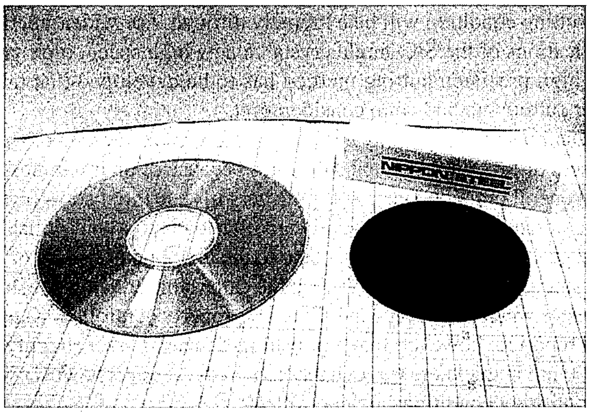


**Fig. 2 3-inch diameter SiC single crystal wafer (6H polytype) Nippon Steel developed, side by side with compact disc**

bining an induction heating simulator accounting for a high temperature strong heat radiation field with internally accumulated experimental and empirical database of the SiC single crystal growth.

A hot zone for growing large size crystals based on predictions obtained through simulations was designed and success was achieved in obtaining a SiC single crystal diameter of 3 inches as a result. **Fig. 2** is a photograph of a 3-inch diameter SiC single crystal wafer (6H polytype) that was manufactured by Nippon Steel.

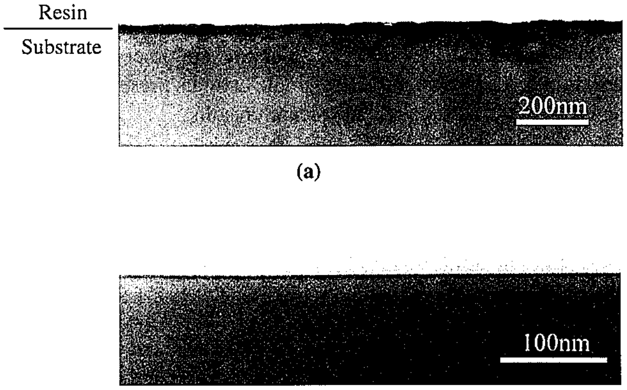
## 3. Machining Techniques of SiC Single Crystal (Substrate Manufacturing Techniques)

Machining techniques (substrate manufacturing techniques) of the SiC single crystal are those employed for manufacturing wafers having desired surface crystal orientation from a SiC single crystal, and are indispensable for practical application of the SiC single crystal to semiconductor devices. In view of the application to semiconductor devices, the substrate manufacturing techniques are evaluated in the following two criteria: (1) shape and dimensional accuracy of the substrate; and (2) crystallographic integrity in the substrate surface. Device manufacturing processes require item (1). Item (2) has a large influence on the integrity of an epitaxially grown thin film. Furthermore, the productivity and costs of the entire substrate manufacturing processes have to be given due considerations from the viewpoint of practical use of the substrates.

The substrate manufacturing processes are divided into cutting processes and polishing processes. Cutting loss, speed, substrate shape and surface damage are among the criteria important for evaluating the cutting processes. Inside diameter (I.D.) blade cutters or wire saws have been used for cutting Si or GaAs semiconductor single crystals but, since SiC single crystal has a hardness second only to diamonds, these cutting methods are inapplicable to SiC without modifications.

At present, the SiC single crystal is cut generally with outside diameter (O.D.) blade cutters, for which diamond-bonded blades can be used[5]. Since the abrasive grain layer thickness of a diamond-bonded blade can be made large, when outermost grains fall out during cutting, new grains appear to the surface as bond is scraped off, and thus hard materials like SiC can be cut stably. Because the stiffness of a blade of the O.D. blade cutters is secured by making its base metal thick, however, cutting loss inevitably increases. What is more, while an adequate cutting thickness is considered as up to 10 times the blade thickness, when cutting a SiC single crystal 2 to 4 inches in diameter, the cutting thickness will be several times to several tens of times larger than the adequate cutting thickness and, hence, the cutting condition will be extremely difficult. For wider practical applications of the SiC single crystal, a new high speed, high yield and high precision cutting method has to be developed that takes other cutting methods into consideration.

Diamonds are generally used as abrasive grains for the polishing process of SiC single crystal substrates because of their hardness. It is a general practice to use soft polishers in sequential steps from a large polishing load to gradually smaller loads to avoid polishing damage. Application of this scheme to the diamond polishing of the SiC single crystals is effective to some extent for reducing polishing damages when polishing conditions are properly controlled. Kanaya et al reported, however, that a polishing-damaged layer roughly 50 to 100 nm in thickness is inevitably left on the surface, however well the polishing conditions are controlled[6].



(a)

(b)

**Fig. 3 Sectional TEM micrographs of**
**(a) (0001) Si surface of 6H-SiC polished with diamond 1.6 nm in roughness**
**(b) (0001) Si surface of 6H-SiC polished by CMP with colloidal silica after surface oxidation**

The so-called chemomechanical polishing (CMP) methods are usually employed for obtaining a damage-free, dead flat surface suitable for fabrication of semiconductor devices. CMPs using colloidal silica or chromium oxide have been tried on SiC, but the methods are not regarded practically promising, since a sufficiently high polishing speed has not been achieved owing to the hardness of the SiC single crystal. To solve the problem a new polishing method combining surface oxidation with the CMP[7] was worked out wherein a surface having a polishing-damaged layer as a result of the diamond polishing is oxidized with water vapor for 3 hours at 1,150°C and is then polished by the CMP using colloidal silica (2 hours with a colloidal silica polishing liquid of a standard concentration of pH10 available in the market). Most of the polishing-damaged layer originally about 50 nm in thickness is changed into an oxide film by the oxidation and is easily removed by the CMP. What remained of the polishing-damaged layer is thin enough to be removed also by the slow CMP.

**Fig. 3** (b) is a sectional TEM photograph of a substrate surface polished by the oxidation + CMP method, and Fig. 3 (a) another of a comparative surface polished only with diamond. As is clear in the figure, the work-damaged layer on the substrate surface not removed by the diamond polishing was removed by the oxidation + CMP method. A surface roughness of Ra = 1.6 nm obtained by the conventional diamond polishing was improved to Ra = 0.4 to 0.8 nm by the developed polishing method[7, 8].

## 4. Crystal Defects and Reduction Thereof

The most serious problem of the SiC single crystals presently manufactured is a defect called micropipe. It is a hollow tube-shaped defect several µm in diameter penetrating the crystal and is replicated into an epitaxial film grown on the crystal surface, constituting a fatal defect for a SiC device, especially for a large current power device[9]. **Fig. 4** is a SEM photograph of a micropipe. The large hexagonal pit is an etch pit formed by molten KOH etching, and a micropipe 2 to 3 µm in diameter is seen at the center of the etch pit. The latest research discovered that the defect is a hollow core dislocation, the occurrence of which Frank predicted theoretically in 1951[10]. The hollow core dislocation is formed when Burgers vector of a dislocation is so large that the dislocation core becomes unstable[11].

Tsvetkov et al classified the causes of micropipes into three

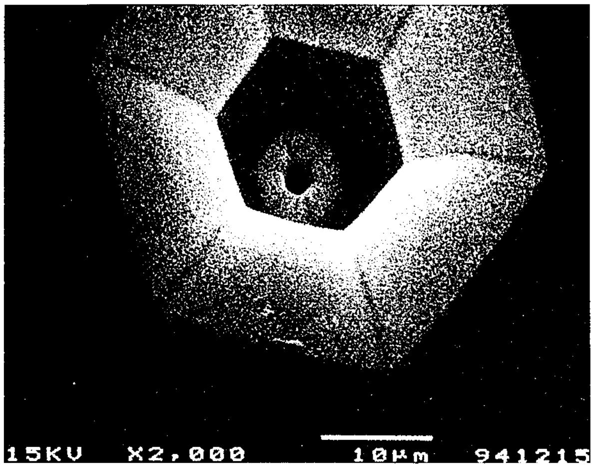


**Fig. 4 SEM micrograph of micropipe**
The hole 2-3 µm in diameter in the center is a micropipe.

groups: thermodynamic, kinetic and technological[12]. The thermodynamic and kinetic causes include thermal strain, three-dimensional nucleation, etc., and the technological causes include process instability, contamination and the like. Ohtani et al, in contrast, attribute the cause of the micropipes mainly to inclusions of foreign polytypes during crystal growth[13]. Non-basal plane interfaces between different polytypes accommodate crystallographic imperfections, which are relaxed during crystal growth into formation of the micropipes. **Fig. 5** is a micrograph of a 6H-SiC single crystal at a section along the crystal growth direction observed with a transmission optical microscope. Here, micropipes are seen to form triggered by inclusion of a foreign polytype (15R) occurring during crystal growth.

Some models of micropipe formation mechanisms have been proposed and they can be classified into two large groups. One is a model to suppose that a micropipe forms as a result of dislocations trapped in a pit or void occurring on a crystal surface[14, 15], and the other is a model to assume that a dislocation having a large Burgers vector is formed in the first place and then its core becomes hollow to form a stable micropipe[16, 17]. In the former surface model, it has been pointed out that formation of macrosteps on the crystal growth surface plays a significant role[14]. Understanding of behaviors of the steps on the single crystal growth surface is essential also in understanding the SiC single crystal growth mechanisms[18]. In the latter model the key issue is how the dislocation having a large Burgers vector forms. With regard to this, some models have been reported such as the one to suppose involvement of twist-type low angle grain boundaries[16] and another to suppose a stacking fault cluster acting as an initial core in the micropipe formation[17]. Future clarification is awaited as to whether any one of the above is correct or more than one mechanisms are involved in the micropipe formation.

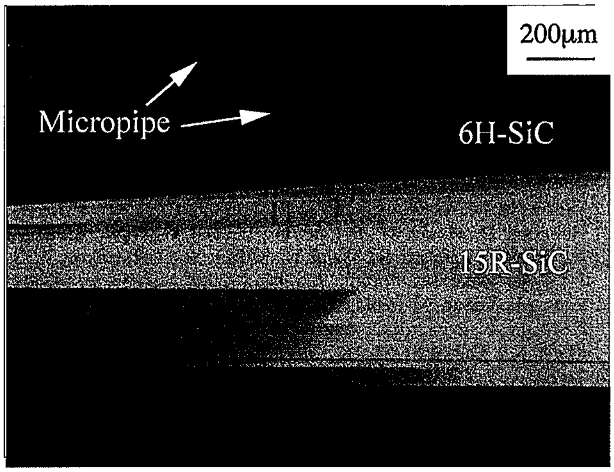


**Fig. 5 Occurrence of micropipe caused by polytype inclusion**
A 6H-SiC single crystal cut along the growth direction is observed with a transmission optical microscope. Micropipes are seen to form triggered by inclusion of a growing foreign polytype (15R-SiC).

From the defect physics and industry viewpoints, an interesting characteristic of the micropipes is their dissociation. Latest studies have clarified that micropipes follow a cycle of formation, propagation and dissociation during the course of crystal growth[13, 19]. Viewed from a standpoint of elasticity theory, a dislocation with a large Burgers vector of n*c* (where *c* is the smallest translation vector) is energetically unfavorable compared with a distribution of number n of dislocations each having a Burgers vector of *c*. This seems to hold true with the micropipe, which is a kind of dislocation, though with a hollow core.

Despite the above, the micropipes appear to exist in a stable state in the SiC single crystal and propagate steadily through a growing crystal. This implies that there exists a large kinetic energy barrier in the dissociation process of a micropipe such as the one shown in **Fig. 6** wherein a micropipe having a Burgers vector of n*c* dissociates into a micropipe having a Burgers vector of (n-1)*c* and a screw dislocation having a Burgers vector of *c*[20]. It has been pointed out that elementary processes on the crystal growth surface play significant roles in the dissociation process[21]. The kinetic energy barrier can be reduced by optimizing the growth conditions of the SiC single crystal and, thus, the dissociation of the micropipe can be accelerated. The micropipe density by this method over the past few years has been reduced and a density of a few micropipes per $\text{cm}^2$ [22] has been attained.

While the occurrence of micropipes has been reduced, it has been made clear that other crystallographic defects have also to be decreased for commercial application of the SiC substrates. X-ray rocking curve measurement, reciprocal lattice space mapping and other methods are being employed to investigate mosaic structure of the modified-Lely grown SiC single crystals[23]. It has been generally reported that, by the X-ray rocking curve measurement, multiple peaks (over several hundreds of arcseconds) and asymmetry of the rocking curves appear in different portions of a crystal. Also reported is a

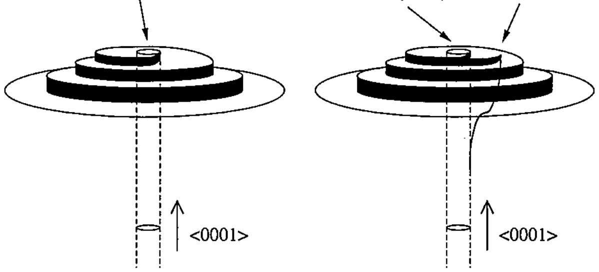


**Fig. 6 Schematic illustration of micropipe dissociation process**
A micropipe dissociates into a micropipe having a smaller Burgers vector and a screw dislocation.

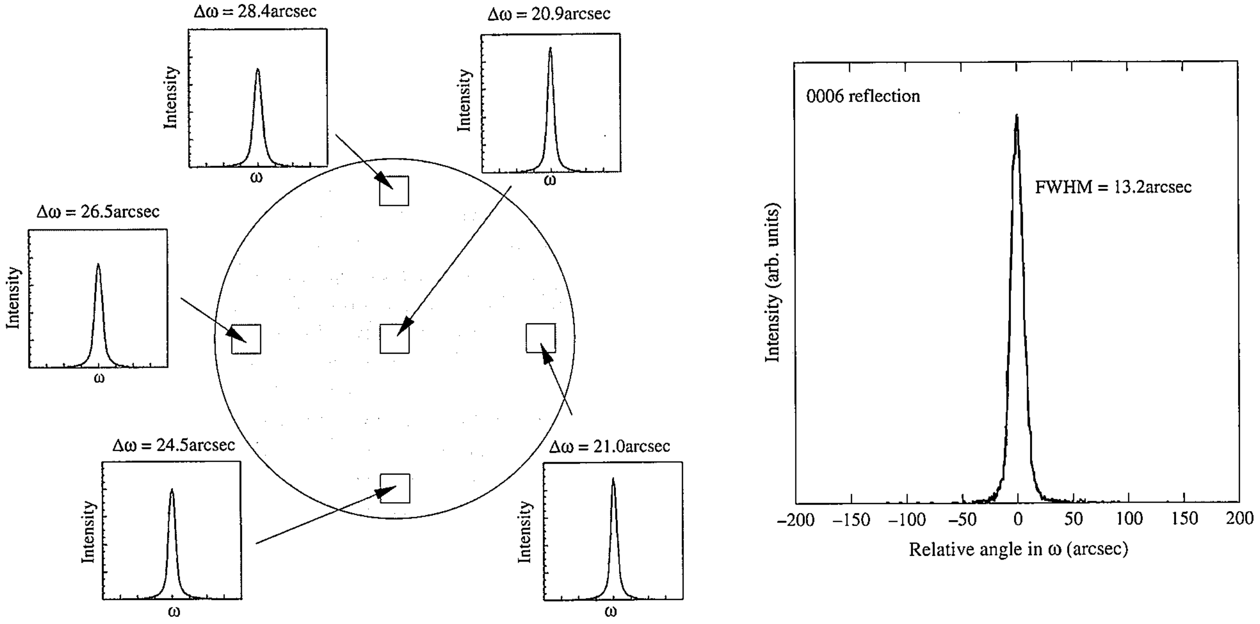


**Fig. 7 SiC single crystal having small mosaicity**
X-ray rocking curves each having a narrow single diffraction peak were obtained across the entire wafer. The full width at half maximum (FWHM) at portions of very good crystallinity is nearly equal to the resolution of the measuring apparatus (right).

correlation between the mosaic structure and warpage and other problems of wafers[24]. Elimination of the mosaicity is essential for the commercial application of the SiC substrates.

Through a series of X-ray rocking curve measurements of SiC single crystal wafers in the market, Glass et al.[23] discovered a good correlation between the micropipe density and the number of multiple peaks of X-ray rocking curves (mosaicity) and, based on this finding, attributed the mosaicity of the SiC single crystals to the micropipe. Other groups of researchers proposed models to suppose that twist type subgrain boundaries (low angle grain boundaries) originating from interactions of growth spiral steps were the cause of the mosaicity in the (0001) plane of SiC single crystals[16, 19]. Katsuno et al. on the other hand, proposed that polytype inclusion was the cause of the mosaic structure and observed a tilt type structure as a variety of the low angle grain boundary structure. They reported that the mosaicity in the (0001) plane of the SiC single crystal was not caused by the micropipes or screw dislocations but by edge dislocation arrays tilted from the *c*-axis[25].

A high quality seed crystal and an optimum temperature distribution in the crystal growing space are considered essential for improving the mosaic structure[26]. Through improvements in the crystal growing hot zone and repeated enlargements of a seed crystal portion having good crystallinity, the authors have recently succeeded in obtaining SiC single crystals showing single-peak X-ray rocking curves with an excellent full width at half maximum (FWHM) of 30 arcseconds or less (spot size: 2 mm × 2 mm) across the entire 1-inch wafer as shown in **Fig. 7**[27].

## 5. Closing

Present state of development activities of SiC single crystal substrates was delineated above focusing on Nippon Steel's development results. The diameter of the SiC single crystal has been enlarged to exceed 2 inches and the occurrence of micropipes has been dramatically reduced. Many high performance SiC devices beyond the limits of the Si devices have been developed and some of them, the Schottky barrier diode for example, are already close to commercial application. It is hoped that application and commercialization of these devices will create markets for the SiC devices and single crystal substrates, which, in turn, will spur further enlargement and quality improvement of the SiC single crystal substrates. It is expected that Nippon Steel's development results will contribute to the creation of markets.

## 6. Acknowledgements

Some of the researches herein presented were sponsored by New Energy and Industrial Technology Development Organization (NEDO) as a part of the "Research and Development on Combustion Control for Energy Conservation" under the Scheme for Important Regional Technology Development of the Ministry of International Trade and Industry (reorganized as the Ministry of Economy, Trade and Industry). The authors are grateful for all the supports and help extended by the related people.

### References

1) Tairov, Yu. M., Tsvetkov, V. F.: J. Cryst. Growth. 43, 209 (1978)
2) Hobgood, D., Brady, M., Brixius, W., Fechko, G., Glass, R., Henshall, D., Jenny, J., Leonard, R., Malta, D., Müller, St. G., Tsvetkov, V., Carter Jr., C. H.: Mater. Sci. Forum. 338-342, 3 (2000)
3) Pons, M., Anikin, M., Chourou, K., Dedulle, J.M., Madar, R., Blanquet, E., Pisch, A., Bernard, C., Grosse, P., Faure, C., Basset, G., Grange, Y.: Mater. Sci. Eng. B 61-62, 18 (1999)
4) Tsvetkov, V., Glass, R., Henshall, D., Asbury, D., Carter Jr., C.H.: Mater. Sci. Forum. 264-268, 3 (1998)
5) Yashiro, H., Kanaya, M.: Report of Results in Fiscal Year 1994 of "Research and Development on Combustion Control for Energy Conservation" under the Important Regional Technology Development. NEDO, 1995, p.1
6) Kanaya, M., Yashiro, H., Ohtani, N., Katsuno, M., Takahashi, J., Shinoyama, S.: Mater. Sci. Forum. 264-268, 359 (1998)
7) Kanaya, M., Yashiro, H.: Report of Results in Fiscal Year 1998 of "Research and Development on Combustion Control for Energy Conserva-

tion" under the Important Regional Technology Development. NEDO, 1999, p.27
8) Aigo, T., Yashiro, H.: Report of Results in Fiscal Year 1999 of same. NEDO, 2000, p.11
9) Neudeck, P.G., Powell, J.A.: IEEE Electron Device Lett. 15, 63 (1994)
10) Si, W., Dudley, M., Glass, R., Tsvetkov, V., Carter Jr., C.H.: Mater. Sci. Forum. 264-268, 429 (1998)
11) Frank, F.C.: Acta. Cryst. 4, 497 (1951)
12) Tsvetkov, V.F., Allen, S. T., Kong, H.S., Carter Jr., C.H.: Inst. Phys. Conf. Ser. 142, 17 (1996)
13) Ohtani, N., Takahashi, J., Katsuno, M., Yashiro, H., Kanaya, M.: Mater. Res. Soc. Symp. Proc. 510, 37 (1998)
14) Giocondi, J., Rohrer, G.S., Skowronski, M., Balakrishna, V., Augustine, G., Hobgood, H.M., Hopkins, R.H.: J. Cryst. Growth. 181, 351 (1997)
15) Liliental-Weber, Z., Chen, Y., Ruvimov, S., Swider, W., Washburn, J.: Mater. Res. Soc. Symp. Proc. 449, 417 (1997)
16) Pirouz, P. : Phil. Mag. A 78, 727 (1998)
17) Heindl, J., Strunk, H.P., Heydemann, V.D., Pensl, G.: Phys. Stat. Sol. (A) 162, 251 (1997)
18) Ohtani, N., Katsuno, M., Takahashi, J., Yashiro, H., Kanaya, M.: Surf. Sci. 398, L303 (1998)
19) Glass, R.C., Henshall, D., Tsvetkov, V.F., Carter Jr., C.H.: Phys. Stat. Sol. (B) 202, 149 (1997)
20) Takahashi, J., Ohtani, N., Kanaya, M.: J. Cryst. Growth. 167, 596 (1996)
21) Ohtani, N., Katsuno, M., Aigo, T., Fujimoto, T., Tsuge, H., Yashiro, H., Kanaya, M.: J. Cryst. Growth. 210, 613 (2000)
22) Ohtani, N., Takahashi, J., Katsuno, M., Yashiro, H., Kanaya, M.: Electron. and Commun. in Japan. Part 2. 81, 8 (1998)
23) Glass, R. C., Kjellberg, L.O., Tsvetkov, V.F., Sundgren, J. E., Janzén, E.: J. Cryst. Growth. 132, 504 (1993)
24) Ellison, A., Radamson, H., Tuominen, M., Milita, S., Hallin, C., Henry, A., Kordina, O., Tuomi, T., Yakimova, R., Madar, R., Janzén, E.: Dimaond Relat. Mater. 6, 1369 (1997)
25) Katsuno, M., Ohtani, N., Aigo, T., Fujimoto, T., Tsuge, H., Yashiro, H., Kanaya, M.: J. Cryst. Growth. 216, 256 (2000)
26) Hofmann, D., Eckstein, R., Kölbl, M., Makarov, Y., Müller, St.G., Schmitt, E., Winnacker, A., Rupp, R., Stein, R., Vökl, J.: J. Cryst. Growth. 174, 669 (1997)
27) Ohtani, N., Katsuno, M., Fujimoto, T., Tsuge, H., Aigo, T., Yashiro, H.: Extended Abstracts of the 1st International Workshop on Ultra-Low-Loss Power Device Technology, Nara, Japan, 2000, p.14