NIPPON STEEL TECHNICAL REPORT No. 83 JANUARY 2001

UDC 669 . 782 : 621 . 382

Electrical Characterization of Separation by Implanted Oxygen (SIMOX) Substrates

Keisuke KAWAMURA*1 Atsuki MATSUMURA*1

Abstract

Electrical performance of low-dose separation by implanted oxygen (SIMOX) substrates that are a promising semiconductor material for high speed, low power LSIs was evaluated. It was quantitatively clarified that the dielectric breakdown behavior of buried oxide (BOX) layer in the SIMOX substrate was dominated by Si islands therein. By optimizing the oxygen dose and the internal thermal oxidation (ITOX) process, the size and density of the Si islands can be reduced and a BOX breakdown field of about 8 MV/cm, comparable to that of thermally grown oxides, was attained. The gate oxide integrity of a low-dose SIMOX fabricated with the ITOX process (ITOX-SIMOX) was found to be equivalent or superior to that of the bulk CZ Si substrates.

1. Introduction

Silicon-on-insulator (SOI) technology is quite attractive for advanced LSIs because of its potential for low-power and high-speed, large-scale integrated circuits (LSIs). Separation by implanted oxygen (SIMOX) is one of the leading methods to produce the SOI substrates. The SIMOX substrates are classified into two types. One is high-dose SIMOX1) and the other is low-dose SIMOX2). The high-dose SIMOX substrates are fabricated with an oxygen ion dose higher than 1.5×10^{18} ions/cm^2 to form a continuos buried oxide layer1). On the other hand, the low-dose SIMOX substrates can be fabricated with a reduced oxygen ion dose range of 3×10^{17} to 4×10^{17} ions/cm^2, which is a so-called dose window2). Because the low-dose SIMOX substrates are superior to the high-dose SIMOX substrates in productivity and crystalline quality of the surface silicon layer3), the low-dose SIMOX have attracted a great deal of attention in recent years.

Although the low-dose SIMOX has the above advantage, it requires an improved buried oxide integrity because of its thinner thickness of about 100 nm than that of the high-dose SIMOX and several efforts were performed to overcome this problem. Recently, it was reported that the internal thermal oxidation (ITOX) process4), which creates the thermal oxide layer on the original buried oxide layer at a temperature higher than 1,300°C, can effectively improve the buried oxide integrity. Nippon Steel Corporation (NSC) approved the advantages of the low-dose SIMOX and ITOX technologies stated above and have been developing the low-dose ITOX-SIMOX substrates energetically.

Among the electrical properties of the SIMOX, the dielectric breakdown field of the buried oxide layer and the integrity of the gate oxide layer formed on the wafer by thermal oxidation are the principal concerns. The dielectric breakdown field of the buried oxide layer is the most important specification of the substrates in power device applications. In CMOS-LSI applications, the breakdown field is also desired to have a higher value to prevent the dielectric breakdown of the buried oxide during the device manufacturing process. The gate oxide integrity (GOI) on the SIMOX substrates is also one of the principal concerns in achieving high performance of devices, which must be equivalent to that on bulk CZ Si substrates to achieve an acceptable device yield.

This report presents the evaluation results of the buried oxide dielectric breakdown field and GOI of the low-dose ITOX-SIMOX substrates. At first, the dielectric breakdown behavior of the buried oxide layer was investigated, and it is clarified that the dielectric breakdown of the buried oxide layer is dominated by silicon islands therein. Reduction of the size and density of the silicon islands by

---

[*1] Technical Development Bureau

optimizing the oxygen dose and the ITOX process was tried, which revealed that the dielectric breakdown field of the buried oxide can be improved to about 8 MV/cm, a level equivalent to that of the thermal oxide layer. We also evaluated the GOI of the low-dose ITOX-SIMOX and clarified that the GOI of the low-dose ITOX-SIMOX substrates is equivalent or superior to that of the bulk CZ Si substrates.

2. Dielectric Breakdown and Silicon Islands of Buried Oxide Layer

2.1 Silicon islands

Photo 1 shows the cross sections of SIMOX fabricated by different oxygen ion doses, which were observed by transmission electron microscopy (TEM). The samples with oxygen ion doses of 0.4×10^{18} ions/cm^2 and 1.6×10^{18} ions/cm^2 correspond to low-dose SIMOX and high-dose SIMOX, respectively. From Photo 1, it can be confirmed that particle-shaped inclusions exist in the samples with doses of 0.6×10^{18} and 1.6×10^{18} ions/cm^2. These inclusions are called silicon islands3). In the general case of high-dose SIMOX, the silicon island density is higher than 10^8 cm^{-2} and the presence of the silicon islands can be easily observed by TEM. On the other hand, the silicon island density in the case of the low-dose SIMOX is usually less than 10^6 cm^{-2}, which are difficult to be observed by TEM.

It has been pointed out that the silicon islands may degrade the electrical quality of the buried oxide layer. Among the influences of the silicon islands, it is considered particularly problematic that the localized thinning of the buried oxide layer where the silicon islands exist degrades the dielectric breakdown field. It can be easily predicted that the above degradation of the breakdown field becomes conspicuous in the low-dose SIMOX substrates, because of their thinner buried oxide layer than that in the high-dose SIMOX. For this reason, it seems to be very important for low-dose SIMOX to understand the influence of the silicon islands on the buried oxide breakdown field and to determine the silicon island density quantitatively.

From the above viewpoint, it was tried to analyze in detail the dielectric breakdown mechanism of the buried oxide in low-dose SIMOX, and the method to evaluate the silicon island density using selective ion etching (RIE) was established5, 6). Consequently, a grasping of the quantitative correlation between the dielectric breakdown field and the size and density of the silicon islands was a success. These results are discussed in the following sections. We also tried to reduce the size and density of the silicon islands by optimizing the wafer manufacturing conditions, the results of which are also introdued6).

Implantation energy: 180 KeV

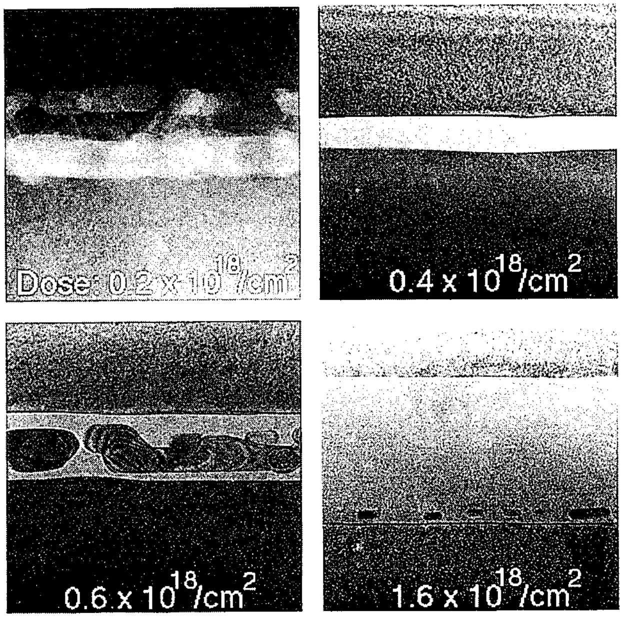

Photo 1 Cross-sectional TEM micrographs of SIMOX wafers manufactured with different oxygen ion doses

2.2 Analysis of dielectric breakdown mechanism of buried oxide layer

Metal-oxide-semiconductor (MOS) capacitors using buried oxide as the dielectric were fabricated on low-dose ITOX-SIMOX substrates. As a reference, MOS capacitors are also fabricated on bulk CZ Si substrates, in which a thermally grown oxide layer of almost the same thickness as that of the buried oxide was used as the dielectric. The structure of a MOS capacitor is shown in **Fig. 1**. Capacitors with electrode areas of 2.5×10^{-7} to 2×10^{-2} cm^2 were periodically formed on the wafer surface. A ramp voltage was applied to each capacitor, and the dielectric breakdown field of the buried oxide was measured for each capacitor.

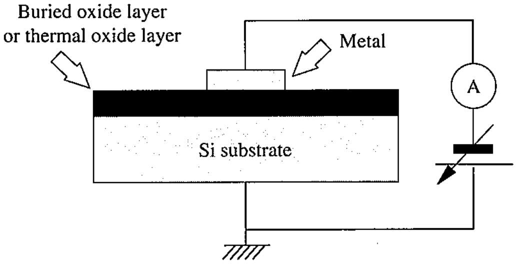

Fig. 1 Structure of MOS capacitor for evaluation of buried oxide layer in SIMOX wafer

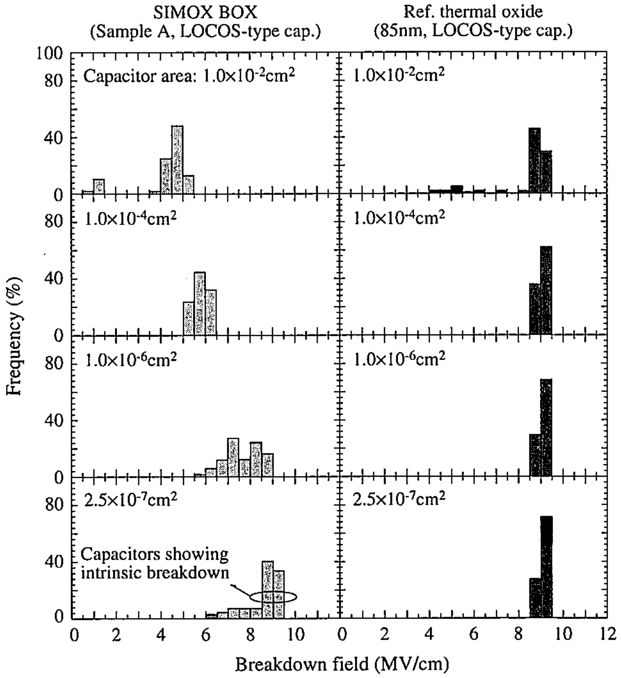

Fig. 2 Dielectric breakdown field histograms of buried oxide and thermal oxide layers in SIMOX wafers

Fig. 2 shows the evaluation results. In this figure, it is shown that dielectric breakdown field of 8 to 9 MV/cm are obtained in the thermal oxide layer, irrespective of the capacitor area. In the case of the SIMOX buried oxide layer, the dielectric breakdown field is about 5 MV/cm for a large capacitor area of about 10^{-2} cm^2 and is lower than that of the thermal oxide layer. This seems to represent the presence of electrically weak portions in the buried oxide layer in the capacitors. As can be seen from Fig. 2, however, the dielectric breakdown field of the buried oxide gradually improves with the decrease in capacitor area. More importantly, at the smallest capacitor area of 2.5×10^{-7} cm^2 in Fig. 2, about 80% of the capacitors exhibit a dielectric breakdown field of 8 to 9 MV/cm, a level equivalent to that of the thermal oxide layer. This result suggests that the electrically weak portions are localized in the buried oxide layer as spot-like defects, which we call electrically weak spots, and that the other portions of the buried oxide layer have electrical properties equal to those of the thermal oxide layer.

In the above situation, the density of the electrically weak spots can be estimated from the capacitor area dependence of the breakdown field shown in Fig. 2. To perform the estimation, it was assumed that the random spatial distribution of the electrically weak spots and the density of the weak spots could be then derived by utilizing the Poisson distribution function as follows$^{6)}$,

$$D(E_{BD}) = -\ln\left(1 - P(E_{BD})\right) / S_{cap} \qquad (1)$$

where $D(E_{BD})$ is the cumulative density of the electrically weak spots exhibiting the dielectric breakdown field between 0 and E_{BD}, S_{cap} is the capacitor area, and $P(E_{BD})$ is failure yield of the capacitors up to the applied field of E_{BD}.

Fig. 3 shows the results of analysis obtained by applying Eq. (1) to the data in Fig. 2. The horizontal axis indicates the electric field applied to the buried oxide layer, and the vertical axis indicates the cumulative density of weak spots. In Fig. 3, the derivable density range of the weak spots varies with the capacitor area, but the weak spot densities derived from different capacitor areas show good agreement, indicating the validity of the above analysis.

2.3 Method for evaluating silicon island density by reactive ion etching

According to the discussion in §2.1, the substance of the electrically weak spots in the buried oxide layer seems to be silicon islands. In order to clarify this point, however, the results for the weak spots in Fig. 3 should be compared with the direct evaluation results of the silicon islands. According to the above motivation, we studied the combination of selective etching by reactive ion etching (RIE) and scanning electron microscopy (SEM) observation as a method for directly observing silicon islands of a low density in low-dose SIMOX$^{7,8)}$. The details of the study are described below.

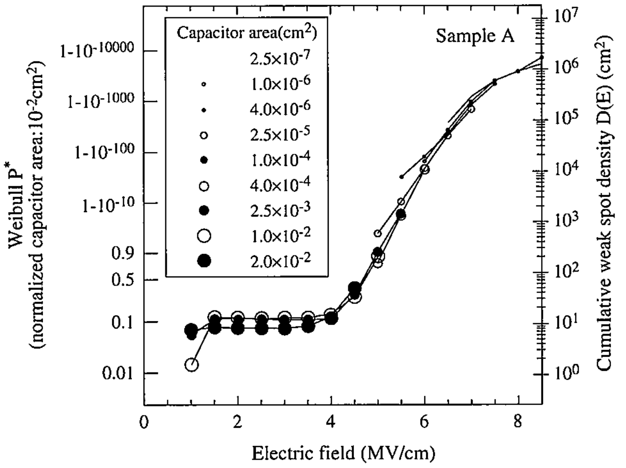

Fig. 3 Relationship between cumulative density of electrically weak spots in buried oxide layer and breakdown field

Fig. 4 shows the schematic diagram of the etching sequence. The selective etching process consists of three steps. In step 1, the surface silicon layer is removed by wet etching or selective RIE. In steps 2 and 3, the buried oxide layer and substrate surface are removed using a selective RIE, respectively. Steps 2 and 3 were performed by anisotropic etching by taking advantage of the characteristics of RIE. After the above etching sequence, a pillar-like structure whose top is covered by SiO$_2$ is formed where each silicon island existed, as shown in Fig. 4(d).

Photo 2 shows the typical observation result of the pillar-like structure by SEM. The pillar-like structure exhibits a clear contrast by the charge-up of the SiO$_2$ and the silicon island density can be derived from the number of charged-up sites in the field of view.

2.4 Density comparison of electrically weak spots and silicon islands in buried oxide layer

To confirm whether weak spots would correlate with silicon is-

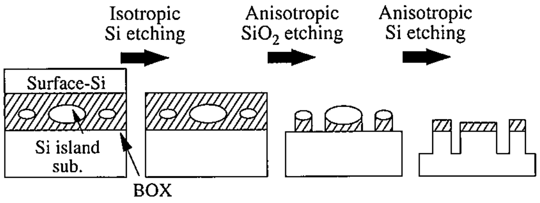

Fig. 4 Etching sequence for formation of pillar-like structure for observation of silicon islands

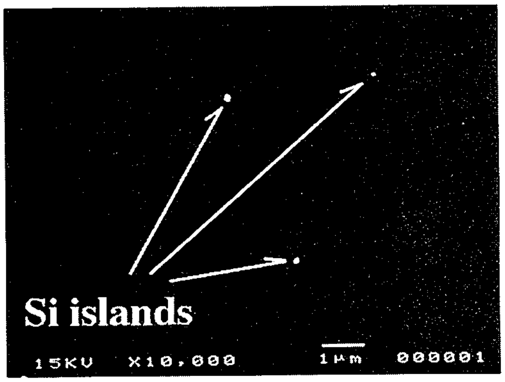

Photo 2 SEM image of silicon islands after etching

Table 1 Buried oxide layer thickness, silicon island density, and electrically weak spot density of SIMOX wafer samples

Sample	BOX thickness (nm)			Si island density by SEM (cm^{-2})	D (8.5MV/cm) (cm^{-2})	Mean breakdown voltage (V)
	Total	Base	ITOX			
A	105	85	20	6.5×10^6	1.7×10^6	- 45
B	116	96	20	1.9×10^7	1.0×10^7	- 40
C	103	83	20	1.0×10^6	6.5×10^5	- 50
D	98	78	20	N.D. ($<10^6$)	7.1×10^4	- 55
E	115	80	35	N.D. ($<10^6$)	2.0×10^4	- 60
F	100	65	35	N.D. ($<10^6$)	4.0×10^1	- 80

lands, the weak spot densities in the six ITOX-SIMOX samples listed in **Table 1** were evaluated and the results were compared to the Si island densities of the same samples which were obtained from the RIE and the SEM observation. The six samples were manufactured by changing the oxygen ion dose or the thickness of ITOX layer to vary the density of silicon islands.

Table 1 shows the silicon island densities of the samples determined by the RIE and the SEM observation, and the total weak spot densities derived from the measurement of dielectric breakdown field. As the value of the total weak spot density, the density of weak spots that exhibited a breakdown field up to 8.5 MV/cm is used. As can be seen in Table 1, the two densities of each sample show in approximate agreement. To make this agreement more clear, the weak spot and silicon island densities obtained from samples A to D, which have the same ITOX thickness, are compared directly in **Fig. 5**. This figure clearly shows a good correlation between the two densities, which indicates that the silicon islands are mainly responsible for the dielectric degradation of the buried oxide layer.

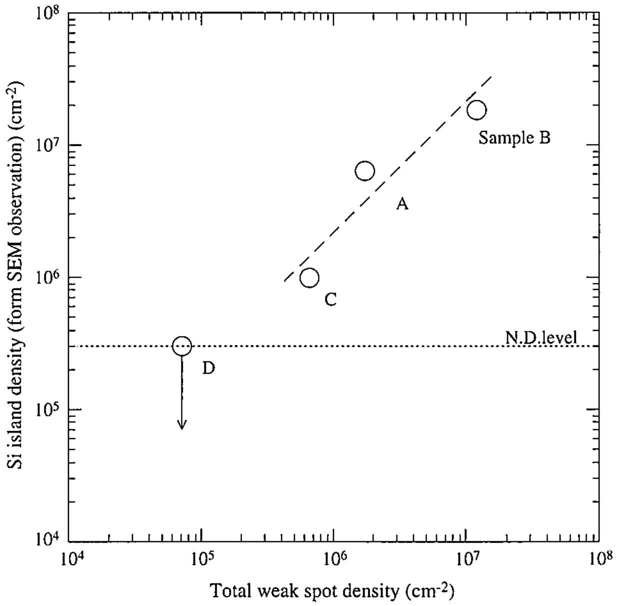

Fig. 5 Comparison of silicon island as determined by SEM and electrically weak spot density in buried oxide layer

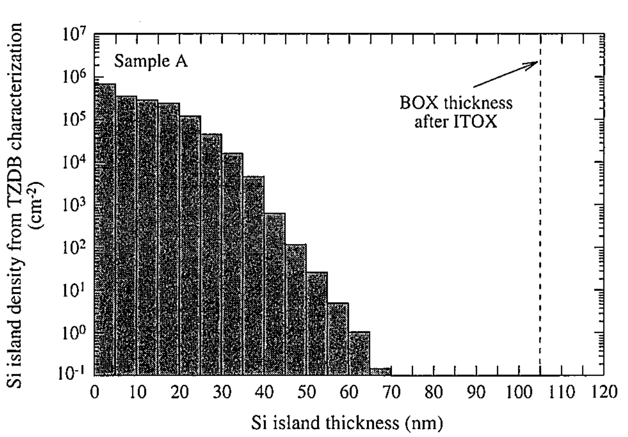

Fig. 6 Distribution of silicon islands in vertical thickness direction as derived from data of Fig. 3 (sample A)

From the electric field dependence of the weak spot density shown in Fig. 3, the size distribution of the silicon islands in the depth direction can be also estimated. This analysis assumes that the buried oxide layer below and above the silicon islands has the same dielectric breakdown field as that of the thermal oxide layer, and that no voltage drop occurs in the silicon islands. Under this assumption, the apparent dielectric breakdown field where the silicon islands exit is given by,

$$E_{BD}^{BOX} = E_{OX}\left(t_{BOX} - t_{Si\ island}\right) / t_{BOX} \qquad (2)$$

where E_{OX} is the dielectric breakdown field where there are no silicon islands, t_{BOX} is the thickness of the buried oxide layer, and $t_{Si\text{-}island}$ is the thickness of the silicon islands in the depth direction. According to Eq. (2), the apparent dielectric breakdown field decreases with the decrease in effective thickness of the buried oxide layer where the silicon islands exist. By applying Eq. (2) to the data of Fig. 3, the dielectric breakdown field along the horizontal axis is converted into the silicon island thickness, so that the density of the Si islands having a certain vertical size can be estimated. The results are shown in **Fig. 6**. In this figure, it is clearly shown that the silicon island density steeply decreases with the increase in silicon island thickness.

2.5 Effects of oxygen ion dose and ITOX layer thickness on dielectric breakdown field of buried oxide layer

From the analysis in §2.2 - § 2.4, the dielectric breakdown field of the buried oxide has been related to the density and size of silicon islands. In this section, we discuss the effects of the oxygen ion dose and ITOX layer thickness on the breakdown field of the buried oxide by utilizing the analytical results. Table 1 shows the buried oxide layer thickness before the ITOX process (base) for each sample. This base thickness is proportional to the oxygen ion dose in principle and can be regarded as an index of the oxygen ion dose.

When we look at the correlation between the base thickness and weak spot density of samples A to D, which have the same ITOX thickness as shown in Table 1, a clear tendency for the weak spot density to decrease with the decrease in base thickness or oxygen ion dose can be found. As described in Section 1, the formation of a continuos buried oxide layer in the low-dose SIMOX wafers is possible in an oxygen ion dose range of about 3×10^{17} to 4×10^{17} ions/cm^2 or what is called a dose window. The above results indicate that the dielectric breakdown field of the buried oxide layer can be increased by setting the oxygen ion dose lower side in the dose window. When the ion dose is reduced below the low end of the dose window, however, many localized leak-defects, so-called pinholes, emerge in the buried oxide layer. This points to the extreme care with which the wafer manufacturing conditions must be set when lowering the oxygen ion implant dose.

The size and density of the silicon islands can also be reduced by the ITOX process. As an example, samples D and E in Table 1, which have almost the same base value but different thickness of ITOX layer, were subjected to the same analysis as in Fig. 6. The results are shown in **Fig. 7**. It was found that the density of the silicon islands in each size are reduced in sample E, which has a larger ITOX layer thickness than sample D. This result suggests that the ITOX process oxidizes the silicon islands to the smaller size and some of the small Si islands before ITOX can be annihilated[9].

As discussed above, it is possible to reduce the number of silicon islands in the buried oxide layer by reducing the oxygen ion dose within the dose window and by increasing the ITOX thickness amount. **Fig. 8** is a histogram of the buried oxide breakdown fields of sample F with the smallest oxygen ion dose and the largest ITOX layer thickness of 35 nm. Although capacitors with a relatively large

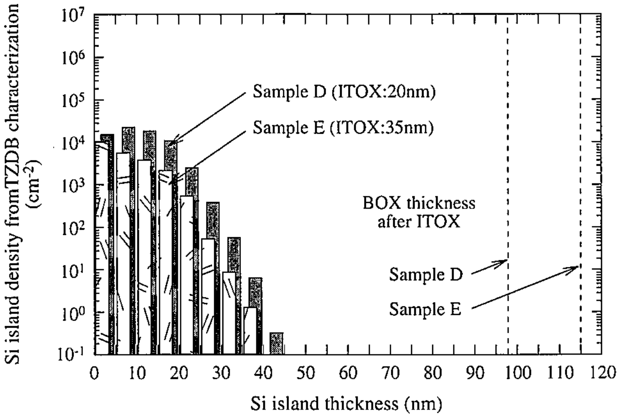

Fig. 7 Distribution of silicon islands in vertical thickness direction in samples D and E as derived by same method as shown in Fig. 6

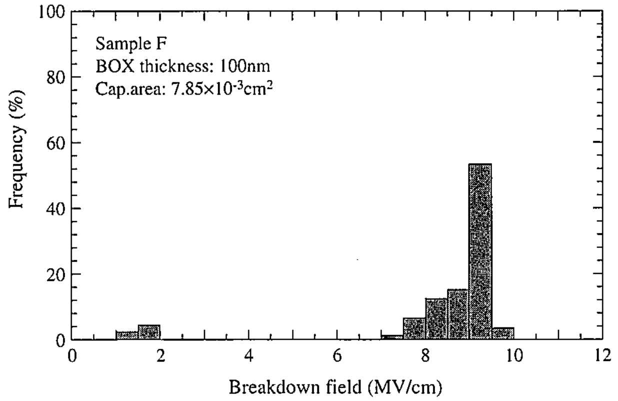

Fig. 8 Histogram of dielectric breakdown field of buried oxide layer in sample F

area of about 8×10^{-3} cm^2 were used in this case, their dielectric breakdown field shows 8 to 9 MV/cm which is equivalent to that of the thermal oxide layer, verifying the validity of the guideline mentioned above.

3. Gate Oxide Integrity Evaluation

Gate oxide integrity (GOI) is generally evaluated by the ramp-voltage breakdown evaluation as described in Section 2 or by time-dependent dielectric breakdown (TDDB) evaluation. The latter method applies to the gate oxide such a constant current that the gate oxide does not show a breakdown immediately, and measures the total amount of charges to the dielectric breakdown of the gate oxide, Q_{BD}. The obtained Q_{BD} can be used for the estimation of the practical service life of LSI, for example.

As described at the beginning of this report, GOI is a property that dominates the performance of LSI, and its evaluation is as important in the SIMOX substrates as in the bulk CZ Si substrates or epitaxial Si substrates. In the case of the SIMOX substrates, however, the buried oxide layer made it impossible to evaluate GOI using the vertical-type devices shown in Fig. 1.

From this standpoint, we studied a device structure that would enable the evaluation of GOI on the SIMOX wafers, and succeeded in establishing the device structure. Using the established device structure, the GOI of the low-dose ITOX-SIMOX substrates was evaluated. This chapter outlines the device structure study and introduces the latest evaluation result of TDDB. The results of the ramp-voltage breakdown evaluation are introduced in the overview of SIMOX wafers in this NSTR issue and are omitted here.

3.1 Establishment of evaluation device structure

The evaluation of GOI on SIMOX substrates involves the problem of the inability to utilize a simple MOS capacitor structure as shown in Fig. 1 due to the presence of the buried oxide layer. To avoid this problem, we created and designed a lateral device with ground electrodes provided on the wafer surface as shown in **Fig. 9** and used it for the evaluation.

In this type of device, a large parasitic resistance sometimes occurs in the surface silicon layer just below the gate oxide and affects the GOI evaluation, which essentially depends on the shape of gate electrodes[10]. As an example, **Fig. 10** shows the relationship between the gate electrode area and intrinsic Q_{BD}s of an approximately 9-nm thick gate oxide layer, which were measured by capacitors with square gate electrodes. The Q_{BD} value was measured on many capacitors of the same electrode area. The Q_{BD} value of a capacitor that exhibited a breakdown time corresponding to the top 20% of the capacitors was adopted as the intrinsic Q_{BD} value.

Generally, when MOS capacitors of such a simple structure as shown in Fig. 2 are formed on a bulk CZ Si or epitaxial Si substrates and are evaluated for gate oxide TDDB, the intrinsic Q_{BD} values obtained are known to exhibit a slight dependence on the electrode area. Furthermore, it is also known that the dependence of the Q_{BD} values on the electrode area exhibits a linear relationship with a negative slope when those were plotted in log-log scale as shown in Fig. 10[11]. In this figure, however, the Q_{BD} values show some discrepancy and become smaller than the dotted prediction line for the gate elec-

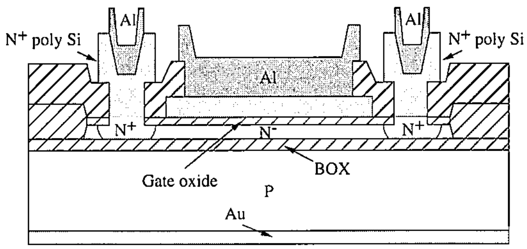

Fig. 9 Structure of lateral device for evaluation of gate oxide integrity of SIMOX wafer

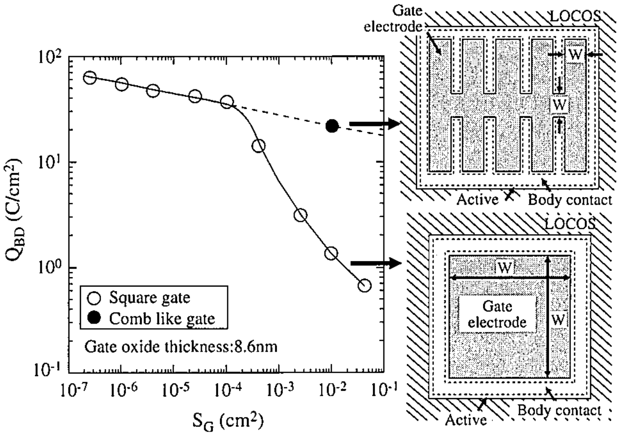

Fig. 10 Gate electrode area dependence of intrinsic Q_{BD} values as obtained from evaluation devices with square and comb-like shaped gate electrodes

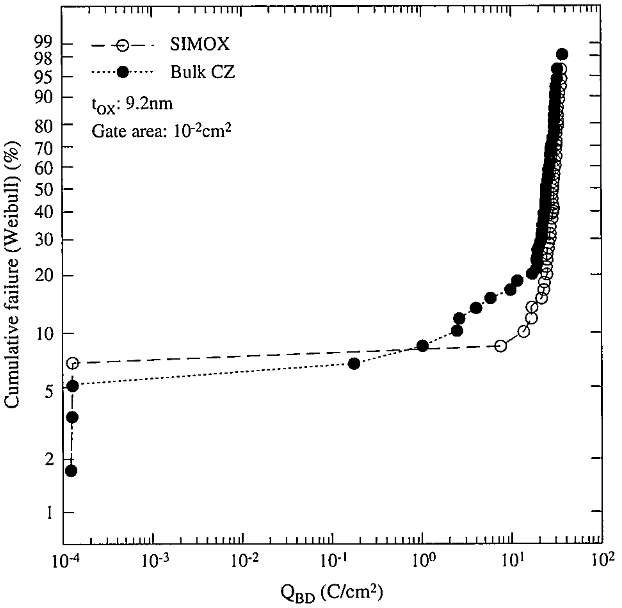

Fig. 11 Q_{BD} **characteristics of gate oxide layers formed on SIMOX wafers and mirror wafers**

trode area larger than 10^{-4} cm^2.

This abnormal Q_{BD} behavior suggests the presence of parasitic resistance in the surface silicon layer, which increases with the increase in electrode area. The acceleration of the gate oxide breakdown shown in Fig.10 can be attributed to the resultant heating or generation of hot electrons at the parasitic resistance portions.

The influence of parasitic resistance noted above can be controlled by using comb-like gate electrodes and making the branch width sufficiently small. Fig. 10 also shows the data of comb-like gate electrodes with a branch width of 20 µm. The gate oxide layer thickness is about 9 nm as is the case with the square gates, and the electrode area is 10^{-2} cm^2. It is clearly shown that the Q_{BD} value obtained from the comb-like gate electrodes show good agreement with the dotted prediction line and that the parasitic effect is controlled regardless of the relatively large gate area of 10^{-2} cm^2. According to the above results, the GOI of the SIMOX is now measured with devices having comb-like gate electrodes with a branch width of 20 µm or less.

3.2 Q_{BD} characteristics of gate oxide layer formed on SIMOX wafers

The Q_{BD} characteristics of the low-dose ITOX-SIMOX substrates measured by using capacitors having comb-like shaped gate electrodes with a branch width of 20 µm are shown in **Fig. 11** as comparison with the bulk CZ Si substrates having the starting material specifications for the SIMOX. The gate oxide thickness is about 9 nm, and the gate electrode area is 10^{-2} cm^2. It was shown that the failure yield (Q_{BD}< 20 C/cm^2) for the SIMOX is lower than that for the bulk CZ Si substrates, which means that the low-dose ITOX-SIMOX substrates have GOI superior to that of the bulk CZ Si substrates. This is probably because some of the grown-in defects originally present on the bulk CZ Si substrates were annihilated or changed into such a form as not to cause the degradation of the Q_{BD} during the high-temperature annealing in the SIMOX manufacturing process.

4. Conclusions

The quality of the low-dose ITOX-SIMOX substrates, which are expected as semiconductor materials for high-speed and low-power LSI applications were electrically characterized. By optimizing the wafer manufacturing conditions, a dielectric breakdown field of about 8 MV/cm for the buried oxide layer in the SIMOX substrates, a level comparable to that of the thermally grown oxide layer, was achieved. The gate oxide integrity (GOI) of the SIMOX substrates was also evaluated and it was clarified that the GOI of the SIMOX is equivalent or superior to that of the bulk CZ Si substrates. These qualities are high enough for the materials in the initial phase of application to mass-production LSI. In these years, the full-fledged use of the SIMOX substrates in cutting-edge LSI is progressing at an accelerated pace. Amid this trend, the improvement of the SIMOX substrates by utilizing the electrical characterization are expected to become more important.

References

1) Izumi, K., Doken, M. Ariyoshi, H. : Electron. Lett. 14, 593(1978)
2) Nakashima, S., Izumi, K. : Electron. Lett. 26, 1647(1990)
3) Nakashima, S., Izumi, K. : J. Mater. Res. 8, 523(1993)
4) Nakashima, S., Katayama, T., Miyamura, Y., Matsuzaki, A., Kataoka, M., Ebi, D., Imai, M., Izumi, K., Ohwada, N. : J. Electrochem. Soc. 143, 244(1996)
5) Kawamura, K., Matsumura, A., Yano, T., Hamaguchi, I., Nagatake, Y., Takayama, S., Tachimori, M., Kurumada, K. : Proc. 1997 IEEE Int. SOI Conf. 1997, p.122
6) Kawamura, K., Yano, T., Hamaguchi, I., Nagatake, Y., Takayama, S., Matsumura, A. : Jpn. J. Appl. Phys. 38, 2477(1999)
7) Nakashima, S., Harada, M., Tsuchiya, T. : Proc. 1993 IEEE Int. SOI Conf. 1993, p.14
8) Nakashima, S. : Private communication
9) Kawamura, K., Nakajima, T., Hamaguchi, I., Yano, T., Tachimori, M. : Proc. 1995 IEEE Int. SOI Conf. 1995, p.156
10) Kawamura, K., Deai, H., Morikawa, Y., Sakamoto, S., Yano, T., Hamaguchi, I., Nagatake, Y., Takayama, S., Matsumura, A., Tachimori, M., Nakashima, S. : Proc. 1996 IEEE Int. SOI Conf. 1996, p.162
11) Degrave, R., Groseneken, G., Bellens, R., Ogier, J. L., Depas, M., Roussel, P. J., Maes, H. E. : IEEE Trans. on Electron. Devices., 45(4), 904(1998)