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Quality Improvement in SIMOX (Separation by Implanted Oxygen) Wafer Technology

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Abstract

Low-dose SIMOX (Separation by Implanted Oxygen) wafers bring high speed and low-power operation of LSIs into reality at low costs. Quality improvement of the SIMOX wafers produced by internal thermal oxidation (ITOX) process was reviewed. The ITOX process increases the thickness of buried oxide (BOX) as well as reduces the thickness of superficial Si layer (SOI layer) to approximately 0.1 μm - a thickness level required for the operation of both the partially-depleted type and fully-depleted type devices - with excellent thickness uniformity across the surface of 200 mm diameter wafers and good reproducibility over production lots. The ITOX process was also found to have positive effects on BOX properties such as pinhole elimination and improved dielectric breakdown performance.

1. Introduction

The rapid progress of information technology in recent years has placed demands on ultra large-scale integration (ULSI) circuits, building blocks of information terminal equipment, for still higher performance improvement. More specifically, achievement of operation fast enough to handle large volumes of information instantly is required. Needs are also mounting for low-power operation to meet the emergence of environmental problems and the penetration of portable equipment. The increasing performance of large-scale integration (LSI) circuits was so far accomplished mainly by the reduction of the design rule that is manufacturing accuracy in LSI fabrication. As the design rule shrank to 0.2 μm or less, however, the in-plane size reduction is about reaching the limit of attaining higher speed, for example. In addition, when the integration density of devices is increased by simple size reduction, the power consumption of LSI circuits increases during operation. Based on these situations, the LSI performance enhancement calls for novel means, apart from extensions of conventional ones.

The silicon-on-insulator (SOI) wafer is expected as a material to break through these limits. The SOI wafer has such a structure that a thin surface silicon layer is dielectrically isolated from the substrate. Devices fabricated in the silicon layer can be operated at high speed and low power consumption. The concept of the SOI wafer was advocated in the 1970s. The advantages of SOI wafers had been recognized, however, high production cost and immature quality of SOI wafers limited their use to special areas such as aerospace or radiation-hardened devices. In the mid-1990s, the limits of present silicon wafer technology became recognized along with the progress in device technology, and the use of SOI wafers in LSI applications was studied in earnest. In the middle of 1998, IBM announced its plan of applying SOI wafer to a multiple processor unit (MPU) for the mass production using the SIMOX (separation by implanted oxygen) wafer, a representative type of SOI wafer. This stimulated other device manufacturers to announce their plan of mass production of SOI devices, which ushered in the SOI era.

The dielectric isolation of SOI wafers usually uses a conventional

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silicon dioxide layer. The silicon dioxide layer may be formed by one of two methods: SIMOX and wafer bonding. The SIMOX process consists of oxygen ion implantation and high-temperature annealing. In the wafer bonding process, two wafers are bonded together through a thermally grown oxide layer, and one of the wafers is thinned afterwards. The wafers produced by the SIMOX process are noted for their excellent surface silicon (SOI) layer thickness uniformity, especially in a thin layer region of 0.1 μm, and are highly expected as wafers suitable for the fabrication of low-power CMOS LSI circuits. Because the SIMOX process is a simple manufacturing process comprising two main steps of oxygen ion implantation and high-temperature annealing, and one SOI wafer can be fabricated from one starting wafer, the SIMOX technology is also expected to ensure low cost at the time of mass production.

Nippon Steel Corporation (NSC) has carried out the research and development of SIMOX-SOI wafers for about 10 years since 1989. Particularly since 1995 when a new ion implanter was introduced, the research and development efforts have been devoted to the realization of quality adapted to mass production. This report gives an overview of the SIMOX wafer technology and introduces the quality improvements achieved recently.

2. SIMOX Wafer Development History

The development of SIMOX wafers originated in the research of Izumi et al.[1] in the 1970s. The SIMOX technology developed then was what is called high-dose SIMOX. Because oxygen ion implantation required a high dose of 1.5 to 2.0×10^{18} cm^{-2}, the dislocation density in the SOI layer was high at about 10^{8} cm^{-2} after the high-temperature anneal. Given this quality problem as well as long ion implantation time and resultant difficulty of cost reduction, the high-dose SIMOX technology was limited to radiation-hard applications and the aerospace field.

In the 1990s, the low-dose SIMOX wafer appeared as a solution to these problems. Because the low-dose SIMOX technology enabled the manufacture of SIMOX wafers with about one-fifth of the oxygen dose required for the high-dose SIMOX wafers, it attracted the notice of semiconductor manufacturers as technology for reducing the production cost of wafers[2]. In the low-dose SIMOX wafers, however, the buried oxide layer decreased in thickness with decreasing dose and there was concern that it would degrade in electrical properties. Internal thermal oxidation (ITOX)[3] is the technology that contributes to improvement in the characteristics of the buried oxide layer, a weak point of the low-dose SIMOX wafer. Use of the ITOX technology slightly increases the thickness of the buried oxide layer, improves its quality at the same time, and allows the buried oxide layer to be formed with satisfactory electrical properties. Based on this improvement, today's mainstream SIMOX wafers are low-dose SIMOX wafers manufactured by using the ITOX technology.

In the above-mentioned technology trend, NSC initiated the research and development of SIMOX wafers in 1989, positioning itself as one of the pioneers in the SIMOX technology field. Simultaneously with the start of the R&D work, the company introduced an NV-200 oxygen ion implanter designed for the mass production of SIMOX wafers from Eaton of the United States[4]. Using the NV-200, research and development of high-dose SIMOX wafers in a diameter range of 4 to 6 inches was carried out, and small amounts of samples as well were shipped. The research target was switched to low-dose SIMOX wafers suited for consumer applications in 1994, and a license for the ITOX technology was acquired in 1995. At the end of 1995, a new ion implanter, Model UI-5000[5], capable of implanting ions into wafers up to 8 inches in diameter was installed from Hitachi. In this way, research and development has been continued and samples of ITOX-SIMOX wafers have been shipped.

NSC now supplies 6-inch and 8-inch ITOX-SIMOX wafers to many customers in Japan and overseas, and holds a leading position in the technology field. In parallel with sample shipment, development work has been carried out and various quality improvements have been accomplished. NSC's ITOX-SIMOX wafer technology and quality improvement are described in the following sections.

3. ITOX-SIMOX Wafer Technology

3.1 Manufacturing process

Fig. 1 schematically illustrates the ITOX-SIMOX process, which consists of main steps of oxygen implantation and high-temperature annealing. Cleaning is performed between the two steps. The technical points of the oxygen ion implantation and high-temperature annealing steps of the ITOX-SIMOX process are outlined below.

3.1.1 Oxygen ion implantation

The oxygen ion dose and substrate temperature are important parameters that govern the initial distribution of oxygen precipitates as source of the buried oxide layer, affecting the formation of a continuous, silicon inclusion-free buried oxide layer. When the implantation energy is 180 keV, the dose range where a continuous buried oxide layer is obtained may be divided into a high-dose region of 1.2×10^{18} ions/cm^2 and above and a low-dose region of 3.0 to 4.5×10^{17} ions/cm^2 [6]. The ITOX-SIMOX wafers introduced here are classified as low-dose SIMOX wafers as already described, and are produced by implanting oxygen ions in the latter dose region. The substrate temperature during implantation should be held high from the standpoint of maintaining crystallinity. A temperature range of 550 to 650°C is employed to obtain a good buried oxide layer with a minimum of current leakage[7].

In CMOS devices using thin-film SOI, it is essential to ensure

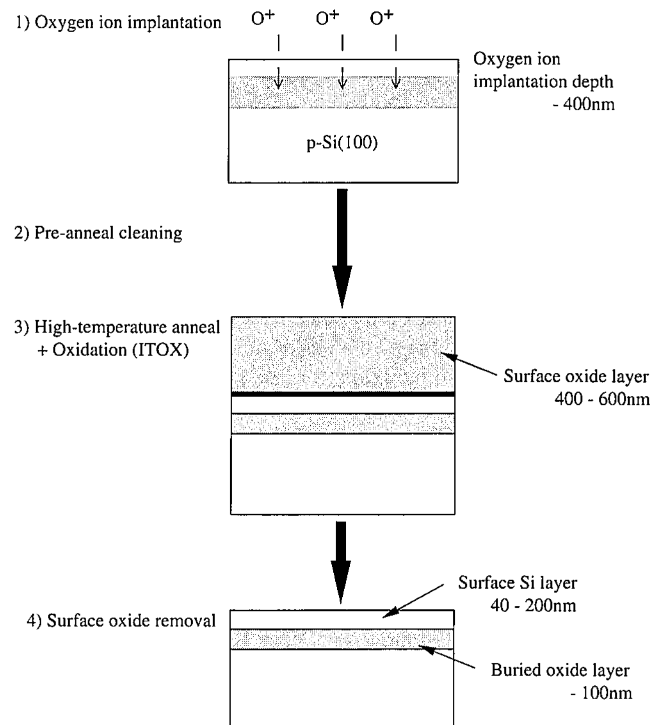


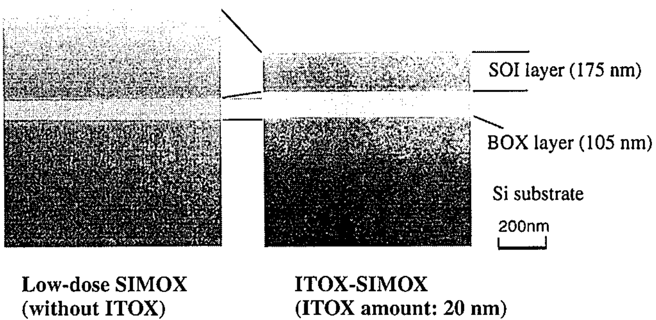
Fig. 1 Schematic of ITOX-SIMOX wafer manufacturing process

film thickness uniformity. To achieve a film thickness uniformity of ±2 nm, it is necessary to control average range of oxygen ions within variation of ±0.5% and the dose of oxygen ions within ±2%. To achieve these severe uniformity requirements, many efforts have been made to maintain the accuracy and stability of the power supply for ion beam acceleration, accuracy of dose measurement, uniformity in ion beam scanning, controllability of channeling, and uniformity in the temperature distribution over a wafer surface during implantation.

Oxygen ion implantation in SIMOX wafer manufacture calls for a dose two to three orders of magnitude higher than ion implantations in device manufacturing. The oxygen ion implanters for SIMOX therefore require a high-current ion beam from the standpoint of throughput improvement. The NV-200 and UI-5000 both use ECR (electron cyclotron resonance) ion sources, and are designed to produce a 100-mA ion beam.

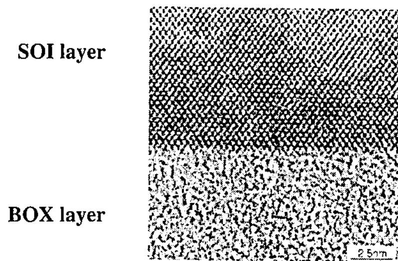
3.1.2 High-temperature annealing

The oxygen-implanted wafer is cleaned by wet process and then annealed at high temperature. This anneal treatment is divided into two steps. In the first non-oxidizing atmosphere anneal stage (1% or less oxygen added to prevent haze), the crystal damages caused by ion implantation are recovered, and a buried oxide layer structure is formed. The latter oxidation stage is what is called internal thermal oxidation (ITOX)[3]. The buried oxide layer is increased in thickness and improved in quality by internal oxidation. At the same time, the SOI layer thickness is reduced by the formation of a thermally grown oxide layer. A high process temperature of 1,300°C or above is used from the standpoints of crystallinity recovery and buried oxide layer quality[7]. In high-temperature annealing in this temperature region, it is concerned that slip may result from the drop in the crystal strength



Low-dose SIMOX (without ITOX) **ITOX-SIMOX (ITOX amount: 20 nm)**

(a) Comparison of wafer without ITOX and ITOX wafer (after surface oxide layer removal)



(b) Enlarged micrograph of SOI layer/BOX layer interface in ITOX-SIMOX wafer

Photo 1 Cross-sectional structure of ITOX-SIMOX wafer (TEM micrograph)

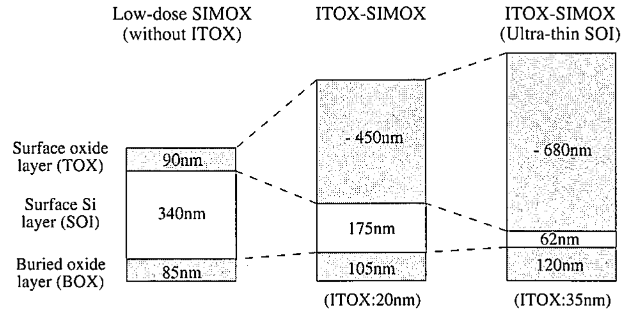


Fig. 2 Relationship of layer structure in ITOX-SIMOX wafers

of silicon. This slip is prevented by devising an appropriate method for holding the wafer.

3.2 Layer structure

Photo 1 shows the cross-sectional TEM image of a ITOX-SIMOX wafer after high-temperature annealing and surface oxide layer removal. The cross-sectional TEM image of a low-dose SIMOX wafer without ITOX is also shown for comparison. The buried oxide (BOX) layer is thickened by the ITOX process, while the SOI layer is thinned by the formation of a surface oxide layer. In the enlarged view (b), a complete lattice image is seen in the SOI layer, and at the same time, the SOI/BOX interface is realized as a steep interface without transition layer. The ITOX treatment is confirmed to be also effective in improving the micro-roughness of the SOI surface and the SOI/BOX interface[8].

The SOI layer thickness can be adjusted by the ITOX oxidation time. **Fig. 2** shows an example of the thickness of each layer obtained when the ITOX time is changed.

4. Quality of ITOX-SIMOX Wafers

4.1 Layer thickness uniformity

The layer thickness uniformity of thin-film SOI wafers is very important especially for the devices with fully depleted operation, because their transistor threshold voltage depends on the SOI layer thickness. **Fig. 3** shows the layer thickness uniformity of the SOI and BOX layers of 8-inch ITOX-SIMOX wafers measured by spectroscopic ellipsometry. Fig. 3(a) shows a 175 nm thick SOI layer for partially depleted operation. The layer thickness uniformity is within ±2 nm. Figs. 3(b) and (c) show 62 and 42 nm thick SOI layers for fully depleted operation, respectively. A good layer thickness uniformity of about ±2 nm is achieved as well as shown in Fig. 3(a). This indicates that a SOI layer thickness of 50 nm or less can be formed by adjustment of the ITOX time alone.

Layer thickness reproducibility is an important quality item in mass production. The SOI layer thickness variation over implantation lots are shown for 8-inch ITOX-SIMOX wafers with a 170 nm thick SOI layer in **Fig. 4** and for 6-inch ITOX-SIMOX wafers with a 62 nm thick SOI layer in **Fig. 5**. Good reproducibility is achieved by strictly controlling both the oxygen ion dose and the ITOX oxidation amount.

4.2 Metal contamination

A SOI layer metal contamination level of less than the lower detection limit of atomic absorption spectroscopy ($\leq 2\times10^{10}$ cm^{-2}) is stably achieved as a result of the measures taken to eliminate contamination in the ion implanters and to increase the purity of tools. Crystal defects existing below the BOX layer of SIMOX wafers are known to have a gettering capability[9], which are also effective to remove metal contaminants in the device manufacturing process.

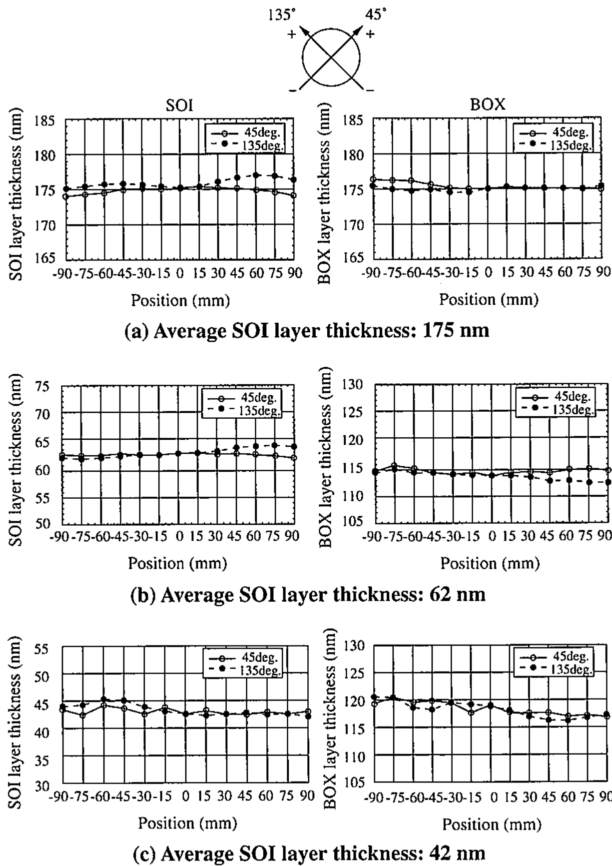


Fig. 3 Layer thickness distribution in plane of 8-inch ITOX-SIMOX wafers

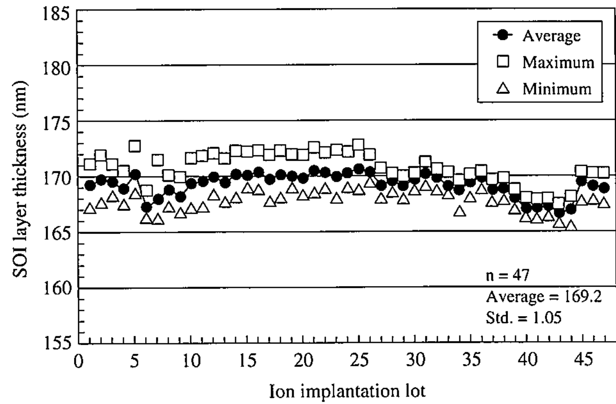


Fig. 4 SOI layer thickness variation over implantation lots in ITOX-SIMOX wafers (8 inches and SOI layer thickness of 170 nm)

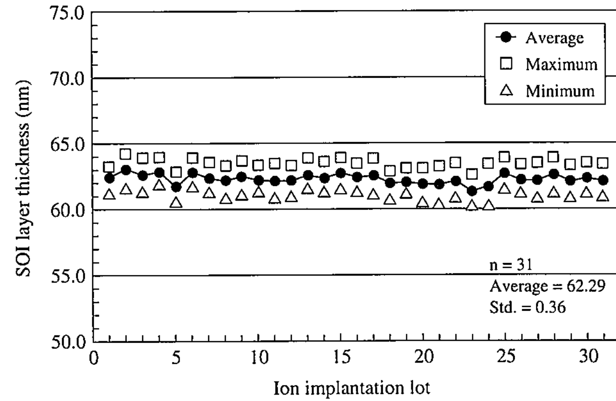


Fig. 5 SOI layer thickness variation over implantation lots in ITOX-SIMOX wafers (6 inches and SOI layer thickness of 62 nm)

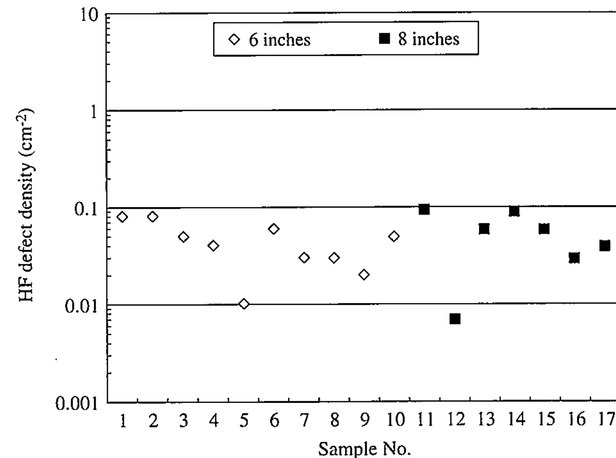


Fig. 6 HF defect density in wafers with 170-nm thick SOI layer

4.3 SOI layer crystallinity

The main crystal defects observed in the SOI layer of SIMOX wafers are threading dislocations and HF defects. Threading dislocations are evaluated by Secco's etching followed by HF treatment. A dislocation density of about 10^3 to 10^4 cm^{-2} is confirmed in the case of low-dose SIMOX. The effect of these dislocations on device characteristics is not clarified yet.

HF defects can be evaluated by immersing a SIMOX wafer in a chemical solution containing hydrofluoric acid (HF), which would etch some defects in the SOI layer and succeedingly the underlying BOX layer as well. The origin of HF defects are reported to be metal silicides[10]. It may be crystal defects such as voids and oxygen precipitates, as observed in bonded wafers[11]. HF defects are known to degrade gate oxide integrity (GOI), so that the reduction in their density is an imperative issue. HF defects are evaluated by immersing in a 25% HF solution for 3.5 h and the density of 0.3 cm^{-2} or less is achieved for our ITOX-SIMOX wafers. Particularly, in a SOI layer thickness of about 170 nm, the specification for partially depleted operation, HF defect density less than 0.1 cm^{-2} is stably accomplished. As an example of evaluation, the HF defect density evaluation results of recent ITOX-SIMOX wafers with a SOI layer thickness of 170 nm are shown in **Fig. 6**. It is evident that an HF defect density of less than 0.1 cm^{-2} is obtained in all samples.

4.4 Quality improvement of BOX layer by ITOX

As explained previously, one of the main problems with low-dose SIMOX wafers is concerned with the electrical properties of the BOX layer. In this section, the quality improvement of the BOX layer by the ITOX process is reviewed.

4.4.1 BOX leakage defects

An important technical issue with BOX layer quality is the reduction in leakage defects. The main cause of BOX layer leakage defects is considered to be the particles adhering to the wafer surface during ion implantation, which interrupt the implanted oxygen ions. The reduction in implanted particles is therefore quite important.

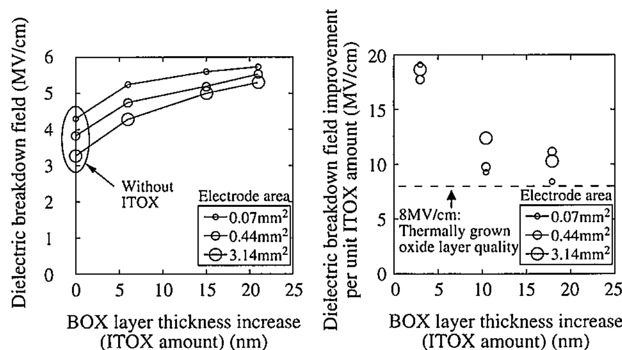
Implanted oxygen ions diffuse to some degree by scattering, so that there is considered to be some size threshold value for particles

that cause leakage defects. In conventional low-dose SIMOX without ITOX treatment, it is pointed out that particles, 0.28 μm and larger in size, can cause leakage defects[6]. In ITOX-SIMOX, it is clarified that some leakage defects are annihilated by internal oxidation[12], and it is possible that leakage defects caused by particles up to 1 μm in size are annihilated by ITOX process in present use. This indicates that the ITOX treatment is effective also in reducing leakage defects.

4.4.2 BOX dielectric breakdown characteristics

Another important issue is the dielectric breakdown characteristics of the BOX layer. It was pointed out that BOX layer of SIMOX wafer is inferior to the thermally grown oxide layer in dielectric breakdown characteristics. Minute silicon inclusions (called silicon islands) in the BOX layer of SIMOX wafer is suggested as probable cause of this degradation[13]. It was investigated that the dielectric breakdown characteristics of the BOX layer in details and quantitatively clarified that the silicon islands are related to the degradation of the dielectric breakdown characteristics[14, 15].

As already explained, ITOX process has the effect of increasing in the BOX layer thickness. In the beginning, this increase in the BOX layer thickness alone was considered to improve the dielectric breakdown voltage of the BOX layer. When the correlation between the ITOX amount and the BOX dielectric breakdown field improvement by the ITOX process was quantitatively investigated, it was found as shown in **Fig. 7** that the dielectric breakdown voltage improvement per unit BOX layer thickness increase (ITOX amount) is much greater than that of the thermally grown oxide layer up to an ITOX amount of 15 nm[12]. This finding indicates the possibility that the ITOX treatment not only thickens the BOX layer but also reduces the size of the silicon islands in the BOX layer or annihilates the silicon islands, as schematically illustrated in **Fig. 8**. These results show that the ITOX treatment is extremely effective in improving the dielectric breakdown voltage of the BOX layer. In fact, these benefits of ITOX are confirmed by the analysis of the silicon island size and density derived from the BOX dielectric breakdown characteritics[15].



(a) Relationship between ITOX amount and BOX dielectric breakdown field **(b) BOX dielectric breakdown field improvement per unit ITOX amount**

Fig. 7 BOX dielectric breakdown characteristics improvement by ITOX

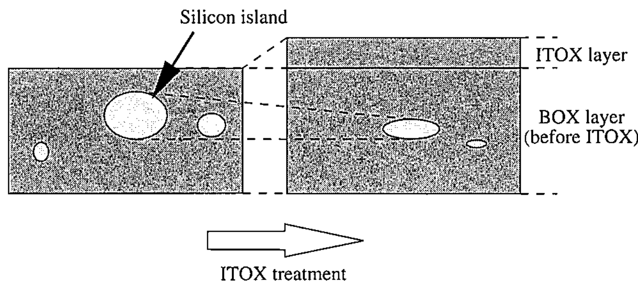


Fig. 8 Schematic of BOX quality improvement by ITOX process

Table 1 Quality of ITOX-SIMOX wafers

Quality item	Quality value	Evaluation method
Layer thickness range (nm)	SOI: 40 - 200* BOX: -100	Spectroscopic ellipsometry
Layer thickness uniformity (nm)**	SOI: ±2.0 BOX: ±2.0	Spectroscopic ellipsometry
HF defects (cm^{-2})	Wafers with 170 nm thick SOI: < 0.1 Wafers with 62 nm thick SOI: < 0.3	
Threading dislocations (cm^{-2})	1×10^3 - 1×10^5	Secco etching
BOX pinholes (cm^{-2})	< 1.0	Copper plating
BOX dielectric breakdown voltage (V)	40 - 80	
Metal contamination ($atoms/cm^2$)	$< 2\times10^{10}$	Atomic absorption spectroscopy (AAS)
Microroughness(R_a) (nm)	SOI surface: 0.4 SOI/BOX interface: 0.5	Atomic force microscopy (AFM)
Warp (μm)	< 30	(200 mm wafers)

*Adjustable according to ITOX treatment time
**In plane of 200 mm wafer

The silicon island density can be reduced by delicately adjusting the ion dose during ion implantation. In samples prepared by keeping the silicon island density low and increasing the ITOX amount, a dielectric breakdown field strength of about 8 MV/cm, comparable to those of the thermally grown oxide layer, and a dielectric breakdown voltage of 60 to 80 V are confirmed to be achievable[14].

For the details of the BOX layer silicon island evaluation and BOX dielectric breakdown improvement, refer to another report[16] in this issue of the NTSR.

4.5 Overall quality

As discussed above, the quality of SIMOX wafers has been improved to a mass-production level by the ITOX treatment. The quality items of recent ITOX-SIMOX wafers are listed in **Table 1**.

5. Gate Oxide Dielectric Breakdown Characteristics

Gate oxide dielectric breakdown characteristics are one of the most important indicators of device operation. **Fig. 9** shows the gate oxide dielectric breakdown characteristics of an ITOX-SIMOX wafer and a bulk wafer which was the starting material of the ITOX-SIMOX[17]. Here the gate oxide thickness was about 24 nm, which was relatively thick value chosen from the standpoint of crystal defect evaluation, the capacitor area was 1 mm^2, the evaluation method was TZDB (time-zero dielectric breakdown), and the dielectric breakdown threshold current was 1 mA. While the bulk wafers develop many B-mode failures, corresponding to dielectric breakdown field of 4 to 8 MV/cm, the SIMOX wafers show no such B-mode failures and exhibit good TZDB characteristics. Grown-in defects like COPs are considered responsible for the B-mode failures in the bulk wafers[18]. High-temperature heat treatment in the SIMOX wafer manufacturing process is considered to annihilate such defects or render

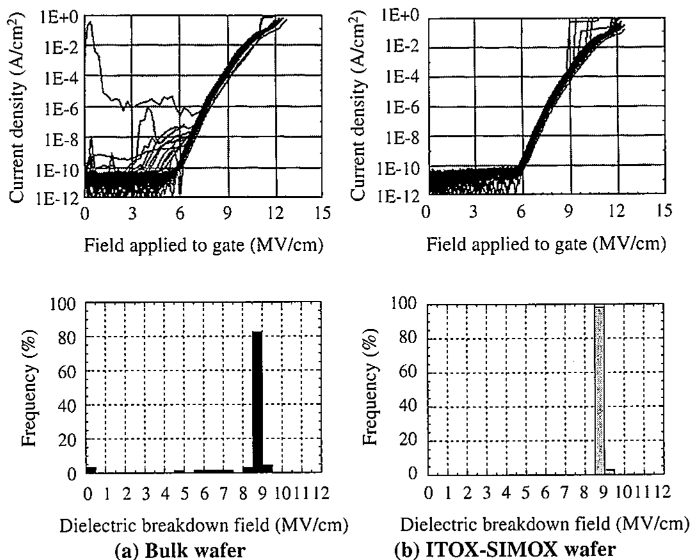


Fig. 9 Gate oxide time-zero dielectric breakdown (TZDB) characteristics
Gate oxide thickness: 24 nm, Electrode area: 1 mm^2, Threshold current: 1 mA

them harmless in the SIMOX wafers.

In the today's actual LSI, gate oxide with a thickness of 10 nm or less is used and its quality is normally evaluated by TDDB (time-dependent dielectric breakdown). For the TDDB evaluation of the SIMOX wafers, refer to another report[16] in this issue of the NSTR.

6. Future Outlook

As explained in this report, the low-dose SIMOX wafers have been improved in quality by technological innovations like the ITOX treatment. About the remaining problems as shown below, we would like to solve as soon as possible.

In terms of wafer quality, it is necessary to reduce BOX pinholes further more. Reducing the number of particles during ion implantation by brushing up on the ion implanters to achieve a pinhole density of 0.1/cm^2 or less is the focal point. Optimization of the annealing process is also expected to contribute to the BOX pinhole reduction. It is considered possible to reduce threading dislocations and HF defects further by improving the manufacturing process conditions. Quality improvement is also expected from the quality adjustment of starting crystals.

As far as the cost reduction is concerned, the SIMOX process can fabricate one SIMOX wafer from one starting wafer as already described, indicating wafer material has no problem for cost issues in principle. Enhancing the productivity of the ion implanters is a key point to the cost reduction, which is under progress now.

7. Conclusions

The ITOX technology has enabled the BOX quality improvement of low-dose SIMOX wafers and provided BOX dielectric breakdown characteristics comparable to those of thermally grown oxide layers. It can also successfully form a ultra-thin SOI layer of about 50 nm and supply high-quality SIMOX wafers for low-power CMOS LSI devices. Mass-production level qualities like layer thickness reproducibility are being achieved. Enhanced coordination with our customers and equipment manufacturers will make further improvements possible and will establish a stable supply system. It is the intent of the authors to launch the mass production of SOI wafers by solving remaining problems as early as possible.

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