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Performance Guarantee of Silicon Wafers by Their Electrical Characterization

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Abstract

Along with the recent rapid advancement of silicon semiconductor devices in terms of higher integration and performance, silicon wafers are required to have increasingly higher performance. The latest design rules of the devices require a precision level in the order of 0.1μm, which fact makes the device fabrication process margin narrower and this, in turn, demands further performance enhancements of the starting material, namely silicon wafers. The main performance indicators of the silicon wafers are the integrity of the now extremely thin gate oxide and a gettering ability effective that is also in low temperature processes. Because device manufacturers ultimately evaluate the performance of the silicon wafers by the fabrication yield of semiconductor chips, evaluation of electrical performance, especially gate oxide integrity, by device measurements is indispensable in wafer development. Since the entry to the silicon wafer business, Nippon Steel has concentrated efforts in developing new generation silicon wafers that match users requirements. Thus, focusing especially on the reliability evaluation, the company introduced a line for manufacturing devices for evaluation, earlier than its competitors in this field of business. This paper describes the silicon wafer properties, the latest device processes demands and the reliability evaluation technologies the company actually implements in the development activities.

1. Introduction

The increasing performance higher integration and speed of silicon semiconductor devices have been basically accomplished by finer device design rules. The reduction in the cell size is known to change the performance of semiconductor devices according to the scaling law.[1)] Assuming that the size reduction of devices is achieved by keeping the electric field constant (or by multiplying all of the MOS transistor gate channel length L, gate channel width W, gate oxide thickness Tox, and supply voltage V by a factor of 1/K), the drive current and delay time decrease by a factor of 1/K, and the device surface area and power consumption decrease by a factor of $1/K^2$. This means that higher density and speed are achieved together with

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lower power consumption. The size reduction of devices actually involved many difficult technological problems, but progressed faster than contemplated by the roadmap (**Table 1**), realizing higher density and speed. The design rules of today's most advanced devices have passed 0.2 μm and are about to reach 0.1 μm.

The required quality of silicon wafers changes with such finer device design rules. For example, device manufacturing process improvements made to comply with these size reduction trends have changed compatibility between processes and silicon wafers, and have made it sometimes impossible to improve the device manufacturing yield with conventional silicon wafers. Generally, the size reduction of devices narrows the margin of their manufacturing processes and makes the performance of silicon wafers as starting materials all the more important.

Generally, the silicon wafer is a perfect crystal totally composed of silicon atoms alone and is often considered to have no development element other than its geometry. Actual silicon wafers are single crystals, but not perfect crystals. Perfect crystals do not always become high-quality wafers. Silicon wafer development competition is still waged in the realization of silicon wafers ideal for specific processes. Especially with the progress of device size reduction in recent years, it has become clear that the presence of grown-in defects (octahedral voids, commonly called crystal-originated particles (COPs)) in Czochralski (CZ) silicon wafers has a serious impact on the reliability of devices. Today, surface COP-free wafers like an epitaxial wafer and a high-temperature annealed wafer are finding expanding markets.

As one recent semiconductor device trend, a change is taking place on a dimension different from the size reduction. Semiconductor device technology development has been mainly driven by semiconductors installed in personal computers, or memories (DRAM) and logic devices (CPU). This trend is changing now. The markets for portable terminals, such as cellular phones and mobile computers, are growing at a phenomenal rate. Furthermore, devices for these portable equipments are leading the technology development.

The performance requirements of such new use are diversifying. For example, lower power consumption is demanded rather than higher speed, or smaller sizes and lighter weights are the priorities. To meet these requirements, the development of flash memory that needs no electric power to retain data in storage and system LSI (or system on a chip (SOC)) that has logic and memory or analog and digital circuits contained on a single chip are rapidly being pursued. These devices delicately differ in the performance requirements of silicon wafers.

The performance of silicon wafers is finally compared and evaluated as the manufacturing yield of semiconductor chips at individual device plants. In the development of silicon wafers, it is indispensable to prepare appropriate evaluation devices and to check and evaluate their performance and reliability. Since the launch of its silicon wafer business, Nippon Steel Corporation (NSC) has led competitors in the construction of a test device process line, particularly emphasized the reliability evaluation of silicon wafers, and carried out its development activities to accomplish next-generation silicon wafers that match the requirements of specific users. This report discusses the main performance requirements of silicon wafers from a device process point-of-view, introduces the techniques the authors have actually practiced for evaluating devices, and refers to the properties required of silicon wafers.

Table 1 Logic device scaling roadmap

Generation	0.25 mm	0.18 mm	0.15 mm	0.13 mm
Mass-production start year	1998	1999	2000	2001-2
Gate oxide thickness	4 nm	3.3-3.5 nm	2.5-3 nm	2-2.5 nm

2. Silicon Wafer Reliability Evaluation Technique

2.1 Reliability evaluation in silicon wafer development

Silicon wafers are used as electronic devices, so that it is indispensable to check the electrical properties of silicon wafers in their development process. The performance of silicon wafers depends on whether or not semiconductor devices with sufficient performance and long life can be manufactured with a high yield after their long manufacturing process, composed of heat, chemical and plasma treatments, among other steps, at individual device manufacturers. The authors prepared a simple device structure on silicon wafers given heat treatment simulating a manufacturing process at a device manufacturer, checked the performance and reliability of the silicon wafers by evaluating their electrical properties, and fed the results back to silicon wafer development. This work mainly centers on the evaluation of gate oxide integrity (GOI), pn junction leakage current, and gettering ability.

2.2 Basic structure of semiconductor devices and performance required of silicon wafers

The basic structure of semiconductor devices and the performance required of silicon wafers are described below by taking as an example the DRAM that is the most popular silicon semiconductor device. **Fig. 1** shows the basic structure of DRAM. The minimum memory storage unit of DRAM consists of one MOS transistor and one capacitor. The MOS transistor works as an on/off switch, and the capacitor plays the role of retaining the charge as storage medium. The charge written (accumulated) in the capacitor is gradually lost due to various leakage currents and must be periodically written before its loss. This operation is called 'refreshing'.

A simple size reduction reduces the capacitance of the capacitor, but the refreshing period cannot be shortened of power consumption. The higher the circuit density, the more the current leakage current must be reduced. To ensure the reliability of devices, it is important from the standpoint of silicon wafer development to ensure the gate oxide integrity of the MOS diodes and to improve the gettering ability to reduce the junction leakage current probably due to wafer bulk defects and metal contaminations.

3. Gate Oxide Integrity (GOI) Evaluation Technology

3.1 Time-zero dielectric breakdown (TZDB) evaluation

Fig. 2 shows the device structures used for gate oxide integrity (GOI) evaluation. The oxidation method, oxide thickness, electrode

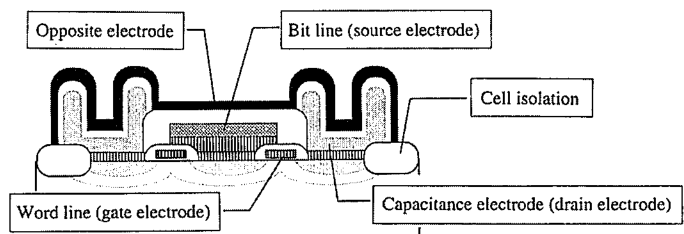


Fig. 1 Basic structure of DRAM

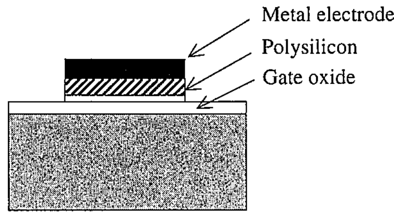


Fig. 2 (a) Structure of polysilicon gate MOS

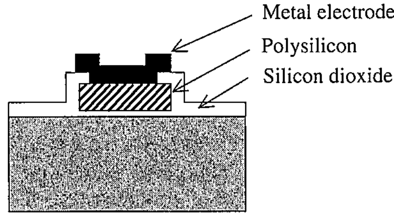


Fig. 2 (b) Structure of polysilicon gate MOS with ultrathin gate oxide

material, and electrode area are changed to suit the specific purposes of evaluation. Most typically, many MOS diodes with an oxide thickness of 25 nm, n+ polysilicon (phosphorus doped), and an electrode area of 20 mm^2 are prepared on the entire surface of a P-type wafer, the I-V curves of the MOS diodes are measured, and the results are statistically evaluated. The oxide thickness of 25 nm, greater than the gate oxide thickness used in actual devices now, is adopted because it is more sensitive for evaluation of COPs in the wafer. To evaluate the effects of smaller defects and surface micro roughness, a thinner oxide layer of about 7 nm is sometimes used. In such a case, the device structure is changed as shown in Fig. 2 (b), so as not to evaluate the effect of damage by the process employed.

Fig. 3 shows the I-V curves obtained when the TZDB of 264 MOS diodes in the plane of a conventional CZ wafer was measured. The current is below the measurement lower limit in the low-electric field region. In the high-electric field region, the Fowler-Nordheim (F-N) tunneling current sharply rises. Unlike in dielectric breakdown, the F-N tunneling current returns to the original level when the voltage is lowered. If there is a defect in its oxide layer, the MOS diode is judged to have had dielectric breakdown when the current suddenly increases at a certain electrical field strength. This dielectric breakdown is judged by two methods. One method is called the low C mode judgment and it evaluates the integrity of gate oxide in the region of 8 MV/cm or less before the F-N tunnel current begins to flow. The other is called the high C mode or D mode and it involves evaluation in the electric field region where the F-N tunnel current flows. The authors set the breakdown criteria at 1 μA/cm^2 for the former method and at 100 mA/cm^2 for the latter method.

Fig. 4 shows the histogram and map of the TZDB test results of the 264 MOS diodes in the plane of the CZ wafer as judged by the high C mode (breakdown criteria of 100 mA/cm^2 or more). The dielectric breakdown (breakdown criteria of 1 μA /cm^2 or more) of the gate oxide is called the A mode dielectric breakdown when it occurs in a breakdown electric field of 1 MV/cm or less, the B mode dielectric breakdown when it occurs in a breakdown electric field of 1 to 8 MV/cm, the C mode dielectric breakdown when it occurs in a breakdown electric field of 8 MV/cm or more, and the high C mode dielectric breakdown (breakdown criteria of 100 mA/cm^2 or more) when it occurs in a breakdown electric field of 11 MV/cm or more. The A mode dielectric breakdown results from oxide pinholes, for example, are mostly attributable to process or clean room environments, including silicon wafer surface particles, and are virtually unobserved in recent clean processes. The B mode is a dielectric breakdown that largely depends on the type and heat treatment of silicon crystals. It was traditionally considered to originate in silicon crystal defects or metal contaminants, but its main cause has been recently identified to be COP. The B mode dielectric breakdown became a serious problem because it occurs in the region where conventional MOS tran-

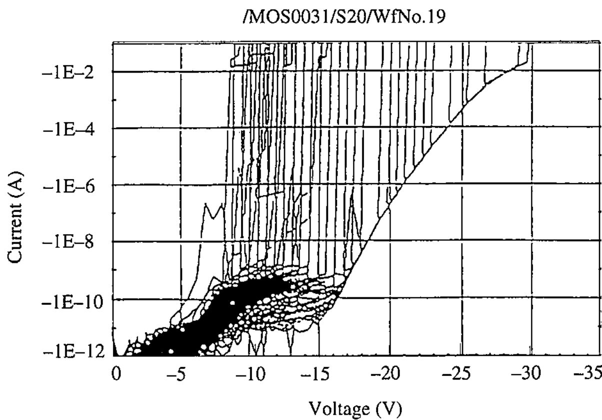
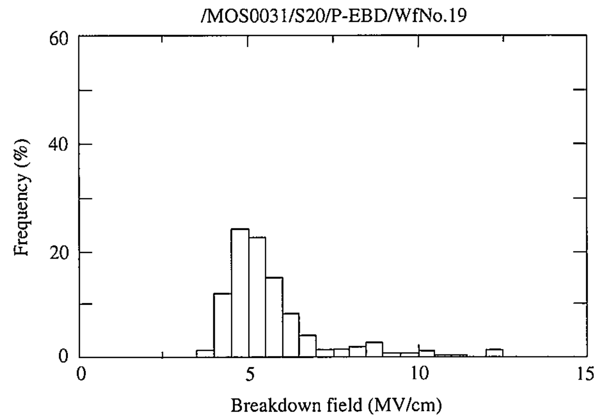


Fig. 3 TZDB measurement results (I-V curves) of conventional polished wafer



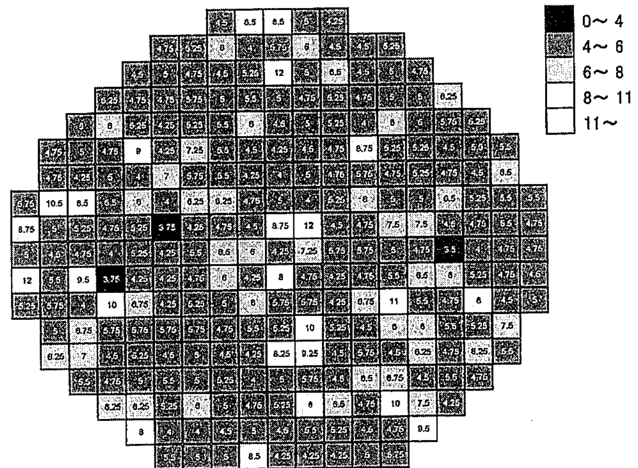


Fig. 4 TZDB measurement results (histogram and map) of conventional polished wafer

sistors are used. This triggered the recent transition to COP-free wafers.

Fig. 5 shows the I-V curves, histogram, and map of the TZDB test results of a nitrogen-doped, argon-annealed wafer with its subsurface COPs annihilated by high-temperature heat treatment. The I-V curves of all 246 MOS diodes overlap until the dielectric breakdown occurs in a high electric field. The annihilation of COPs eliminated the B mode dielectric breakdown, and all MOS diodes achieved a breakdown electric field of 11 MV/cm or more. Very good gate oxide characteristics are obtained. In the flash memories, which have been growing rapidly in recent years, the F-N tunneling current is used for writing to floating gates, so an electric field of about 10 MV/cm is sometimes employed. Reliability in such a high electrical field is required.

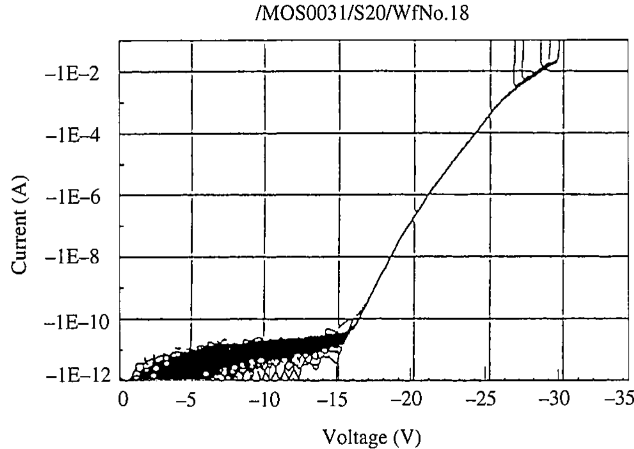


Fig. 5 (a) TZDB measurement results (I-V curves) of argon-annealed wafers

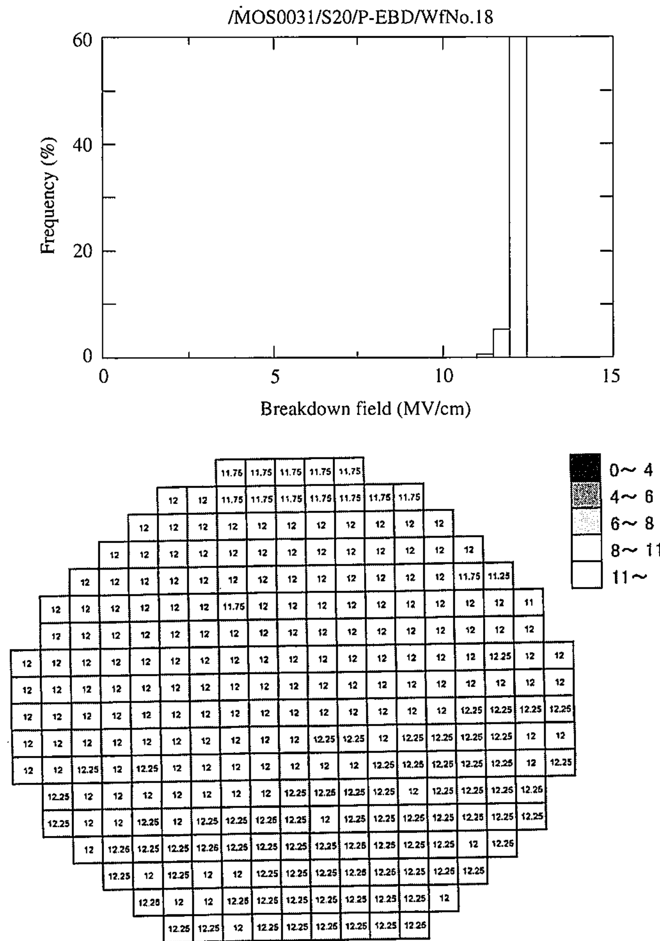


Fig. 5(b) TZDB measurement results (histogram and map) of argon-annealed wafer

3.2 Time-dependent dielectric breakdown (TDDB) evaluation

When the gate voltage is continuously applied to the gate oxide, the gate oxide, which is initially sound, gradually deteriorates and eventually fails. This type of failure is evaluated by the time-dependent dielectric breakdown (TDDB) test. Gate oxide integrity evaluation often refers to the TDDB evaluation. The TDDB technique simultaneously applies a constant stress current (F-N tunneling current) to many MOS diodes formed on a wafer, counts the MOS diodes that fail with time, and measures the time to the failure of the last diode. In the TDDB test, the flow of the F-N tunneling current forms defects in weak portions of the gate oxide, leading to the eventual failure of such weak portions.

Reliability theory analyzes this type of wear out degradation by the Weibull distribution introduced by W. Weibull[2] of Sweden. The Weibull distribution is the distribution derived according to the "weakest link model" that the failure of a device is determined by one of the defects scattered in the device that fails first. An example of TDDB measurement is shown in **Fig. 6**. The time of failure of each cell is plotted along the horizontal axis and is represented by the amount of transmitted charge (Qbd in C/cm^2) multiplied by the current. The vertical axis indicates the cumulative failure probability P by the Weibull function (= ln (– ln (1 – P))). If the dielectric breakdown of the gate oxide is expressed by the Weibull distribution, it follows a straight line with the slope m on a Weibull plot because the reliability function is expressed as $1 - P = \exp(-at^m)$.

Because the slope m assumes a different value for a different breakdown mode, the change in the failure mode can be read from the Weibull plot. Usually, the Weibull plot of Fig. 6 can be divided into the premature failure region (up to 0.001 C/cm^2), chance failure region (0.001 to 10 C/cm^2), and intrinsic failure region (above 10 C/cm^2). The MOS diodes that failed in the premature failure region are

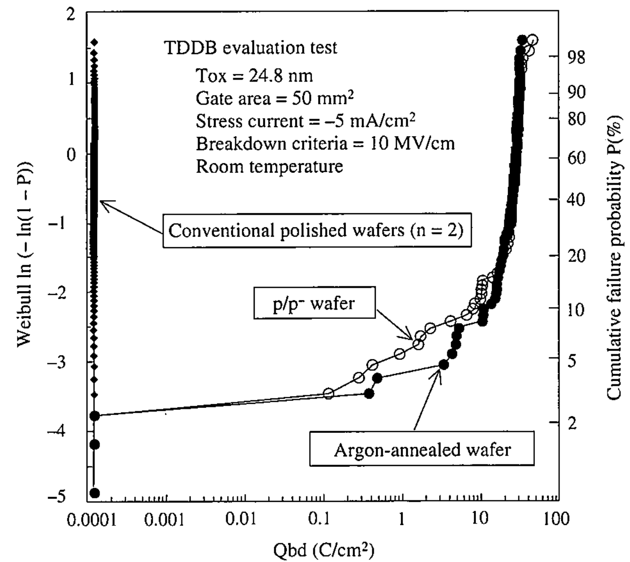


Fig. 6 TDDB measurement results

equivalent to the MOS diodes that failed in the A mode and B mode in the TZDB test. The MOS diodes that failed in the chance failure region are the MOS diodes that did not fail prematurely but eventually failed because of small defects left in the gate oxide that degraded with time. The TDDB evaluation mainly addresses defects in the chance failure region. The intrinsic failure region is the region where the gate oxide fails by wear out degradation.

The TDDB test evaluates the essential quality of the gate oxide in the intrinsic failure region. The TDDB test result may be indicated by the cumulative failure rate at a certain Qbd (e.g., 10 C/cm^2), the cumulative failure rate (proportion of MOS diodes with gate oxide defects) at the boundary between the chance failure region and the intrinsic failure region, or the cumulative failure rate = 1 – exp (–DA) (where D is the approximate defect density in 1cm^2 calculated by defining A as the MOS diode area) from these cumulative failure rates and the MOS diode area. In a flash memory application, the TDDB is an important index in that it evaluates the number of times the flash memory can be written on. The amount of transmitted charge that corresponds to 1 million writes, a substantially acceptable lifetime, is estimated at about 4 C/cm^2.

3.3 Copper plating method

The dielectric breakdown characteristics of the gate oxide are generally evaluated by preparing MOS diodes, as done in the TZDB and TDDB tests. This approach is disadvantageous in that processing and measurement take time. Measurement of MOS diodes cannot accurately indicate what point has failed in the electrode area of a MOS diode, thus making it difficult to isolate and observe failure sites. Copper plating method is proposed by Itumi et al.[3] as a simple method for evaluating gate oxide dielectric failures and identifying failure sites. The copper plating method involves establishing electrodes as shown in **Fig. 7 (a)** for a wafer on which gate oxide is formed and plating copper on the gate oxide surface. When electric current is applied between the substrate and solution electrodes, it flows through the gate oxide only at defects where dielectric breakdown has occurred. Copper particles are precipitated in such dielectric failure sites alone. Evaluation of the wafer with a surface particle counter can determine the density, degree, and position of dielectric breakdown at the same time. This method is very effective in identifying the distribution and position of gate oxide failures.

In 1996, the authors evaluated the gate oxide failure of conventional mirror wafers by the copper plating method, observed by the combination of focused ion beam (FIB) and transmission electron microscopy (TEM) the dielectric failure sites where copper was electrodeposited, and found that COPs were chiefly responsible for the failure of the gate oxide near 4 MV/cm[4] as pointed out by Park et al.[5]. **Fig. 7 (b)** shows the cross-sectional TEM image of a copper-electrodeposited site as observed by the copper plating method. Right below the failure site (copper- precipitated site) exists a twin-octahedral void (COP).

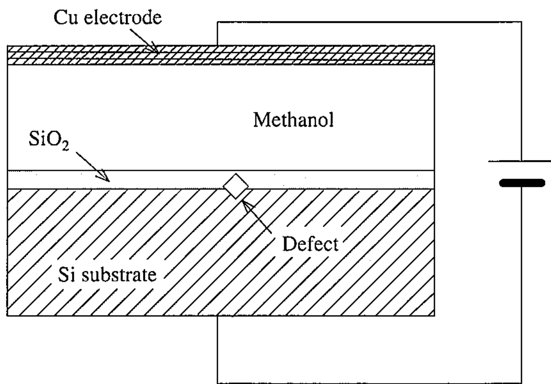


Fig. 7 (a) Copper plating method

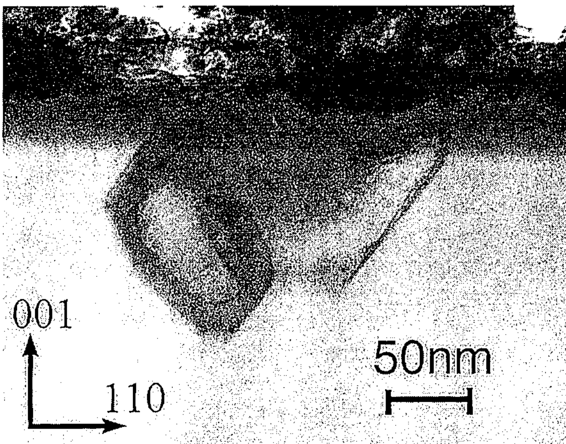


Fig. 7 (b) Cross-sectional TEM image of gate dielectric failure site at which copper was plated

4. Refresh Characteristics Evaluation

4.1 PN junction leakage current evaluation

The gate oxide integrity (GOI) evaluation reflects the quality of the wafer near its surface alone. Because semiconductor devices are fabricated to a depth of about 5 μm from the wafer surface, it is necessary to evaluate not only the surface, but also the bulk of wafers. The refresh characteristics of DRAMs, for example, are influenced by defects and metal impurities in the bulk of wafers. PN junction leakage current is evaluated as one method for evaluating such bulk defects. The pn junction leakage current is an important and basic evaluation item for devices. Causes of this leakage current depend to a large extent on the technology of building the device structure like cell isolation and involve various factors. Little evaluation was made from the standpoint of correlation with crystal defects.

Fig. 8 shows the most basic device structure for the pn junction leakage current evaluation. Surface phosphorus ion implantation and activation heat treatment form a pn junction. Formed on top are an electrode for measurement and a guard ring electrode for applying the voltage to limit the inrush current of minority carries from the surrounding area. Many structures of this type are formed on the

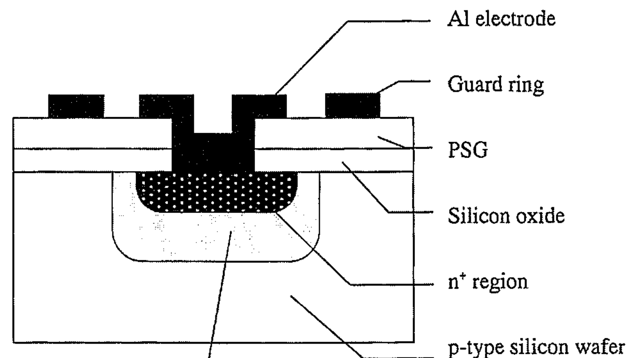


Fig. 8 Device structure for measurement of pn junction leakage current

wafer and used to measure the current (reverse bias current)-voltage characteristics when the pn junction diode is reverse biased. When the depletion layer has no defect, there are observed only currents because of carries (electrons and holes) thermally produced across the band gap Eg and because of the minority carriers diffusing from the substrate. When the depletion layer has a defect, many electrons and holes are generated through the deep level formed in the band gap, increasing the inverse current (generated current). This generated current causes the degradation of refresh characteristics in the device.

In a silicon wafer pulled at a very low rate during crystal formation, it is known that COPs disappear and that dislocation defects (huge dislocation loops) form in their place. Such wafers are known to provide a relatively good gate oxide integrity. When the pn junction leakage current of the wafers was measured, it was found that dislocation defects existing at a density of about $2 \times 10^3/cm^3$ acted as sources of leakage current[6]. Oxygen precipitates in silicon crystals are also known to cause pn junction leakage current.

The authors intentionally formed octahedral or platelet oxygen precipitates at various densities in silicon crystals by changing heat treating conditions, and measured the pn junction leakage current of the silicon crystals to evaluate the effect of oxygen precipitates on the pn junction leakage current (**Fig. 9**). As a result, it was found that the amount of pn junction leakage current per oxygen precipitate varies with the diagonal size of oxygen precipitates, irrespective of the morphology of oxygen precipitates, and is 1E-15 A/precipitate for the oxygen precipitate size of 200 nm and 4E-15 A/precipitate for the oxygen precipitate size of 1,000 nm[7]. It was thus made clear that the oxygen precipitates affect the pn junction leakage current or refreshing characteristics.

In highly scaled-down devices under development now, the electrical capacitance to retain memory is relatively decreased to increase the importance of limiting the leakage current. Defects in the active layer of the device become sources of leakage current themselves. Especially when there are metal contaminants, they are entrapped by the defects to become large leakage current sources. Metal contaminants like iron themselves form deep levels and become leakage current sources. Improvement in reliability against leakage current makes it important to eliminate defects in the active layer of the device and to improve the gettering ability of the substrate as described in the next section.

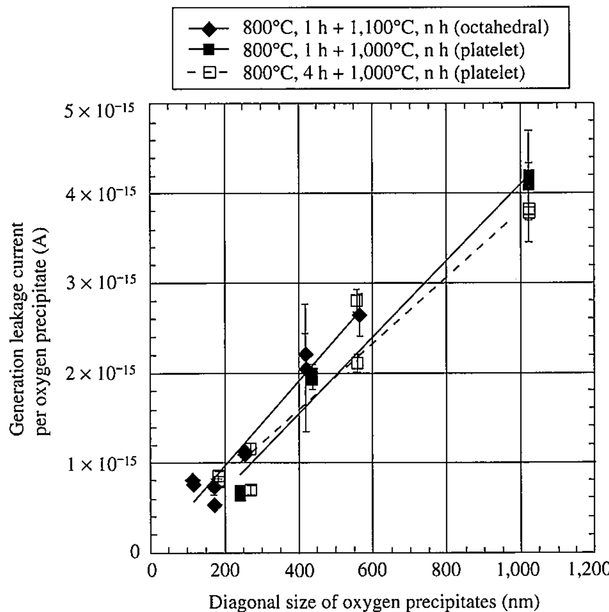


Fig. 9 Relation between oxygen precipitate density and pn junction leakage current

5. Gettering Ability Evaluation

5.1 MOS C-t method (generation lifetime: τg evaluation)

In the device manufacturing process, metal contaminants inevitably enter the silicon wafer from the manufacturing equipment and interconnection materials. Refresh failures that actually occur in the devices are often caused by metal contamination in the device manufacturing process. Heavy metals, although their total amount is trace, accumulate at the gate oxide interface and cell separation points, and sometimes degrade the gate oxide integrity and pn junction leakage current characteristics of the devices. To ensure the reliability of wafers, it is necessary to improve the contamination resistance or gettering ability of the wafers to such a level that the device characteristics are not degraded by a small amount of metal contamination.

One method for evaluating the gettering ability consists of intentionally contaminating a wafer with heavy metals and measuring the aforementioned pn junction leakage current of the heavy metal-contaminated wafer. This method calls for a high-temperature well structure formation treatment to form the pn junction, giving rise to the concern that the gettering ability may change with the treatment conditions. To evaluate the gettering ability of wafers in the condition close to that of wafers at the time of their shipment, the authors used the MOS C-t method (or Zerbst method[8]) that forms an Al-MOS cell with a minimum of high-temperature process steps and measures the time response of the electrical capacitance (C-t) of the Al-MOS cell.

The MOS C-t method is outlined here. When a MOS capacitor is forward biased into accumulation and is then rapidly reverse biased as shown in **Fig. 10**, the depletion layer expands in the silicon, and the electrical capacitance (C) of the MOS capacitor drops below the electrical capacitance (Cox) of the gate oxide alone. The MOS electrical capacitance is set in deep depletion, passes the equilibrium capacitance Cf (electrical capacitance in the condition in which electrons are collected in the inversion layer until thermal equilibrium is reached), and assumes a smaller value. As the minority carriers generated in the depletion layer (electrons in the case of a p-type wafer) gradually collect in the inversion layer toward the thermal equilibrium condition, the depletion layer shrinks again, and the electrical capacitance approaches Cf. This transient response of C can be measured and analyzed to evaluate the generation lifetime (τg) of minority carriers[8].

When evaluating the gettering ability, the Al-MOS structure is formed after intentionally contaminating the silicon wafer with the target metal, and the generation lifetime (τg) is then measured. A good τg value is obtained if the contaminating metal is removed from the active layer (or the depletion layer in this case) by the gettering effect. If the gettering effect is not working, the contaminating metal remains and degrades (or shortens) the generation lifetime τg.

As described in the explanation that follows, epitaxial wafers having gettering ability improved by nitrogen doping have been developed. The evaluation of this gettering ability uses the MOS C-t method. For the purpose of evaluating the gettering ability of the epitaxial wafers with respect to nickel, various wafers were contaminated with about $1E12/cm^2$ of nickel by the spin coat process. Al-

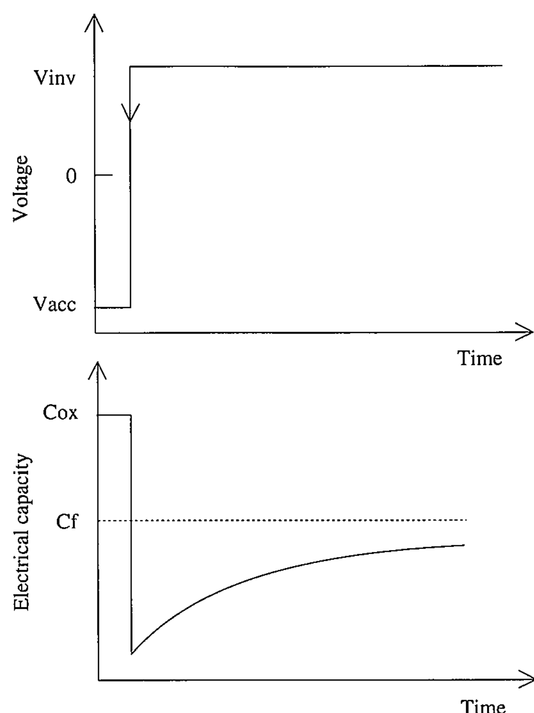


Fig. 10 Change in electrical capacity during MOS C-t measurement

MOS capacitors were fabricated on the wafers, and the minority carrier generation lifetime (τg) of the Al-MOS capacitors were measured. Conventional reference p/p⁻ and p/p⁺ epitaxial wafers have no gettering effect at all with respect to nickel, so their τg deteriorates to 1 μs or less. Epitaxial wafers with the gettering ability of the substrate strengthened by nitrogen doping have a τg of 10 ms or more in both p/p⁻ and p/p⁺ types. The p/p⁻ and p/p⁺ epitaxial wafers are thus confirmed to have a high gettering ability[9].

The authors have been studying the feasibility of producing an epitaxial wafer with a powerful gettering ability right below the epitaxial layer by first forming necessary gettering sites on the wafer by ion implantation and then depositing the epitaxial layer on the wafer. A substrate was dosed with Ar^+, B^+ and BF^{2+} ions to about 1E14/cm², and the epitaxial layer was deposited on the ion-dosed substrate. The epitaxial wafers thus produced were evaluated for the gettering ability with respect to nickel. They are confirmed to have a sufficient gettering effect[10].

5.2 Deep-level transient spectroscopy (DLTS)

Deep-level transient spectroscopy (DLTS) is available as a method for spectroscopically evaluating deep levels in semiconductors due to heavy-metal contamination by measuring the transient response of the capacitance of pn, MOS, and Schottky junctions while changing the temperature[11]. **Fig. 11** shows an example of DLTS signal for iron as a typical contaminating element. The DLTS method is similar to the MOS C-t method in that it measures the transient response of the junction capacitance, but is greatly different from the MOS C-t method in that its transient response time region is 1 sec or less against a few minutes to a few hours for the MOS C-t method. This is because the MOS C-t method observes the way the minority carries thermally generated at deep levels accumulate in the inversion layer, while the DLTS method observes the way the majority carriers packed at deep levels in the accumulation condition are released at the instant the majority carries reach the depletion condition.

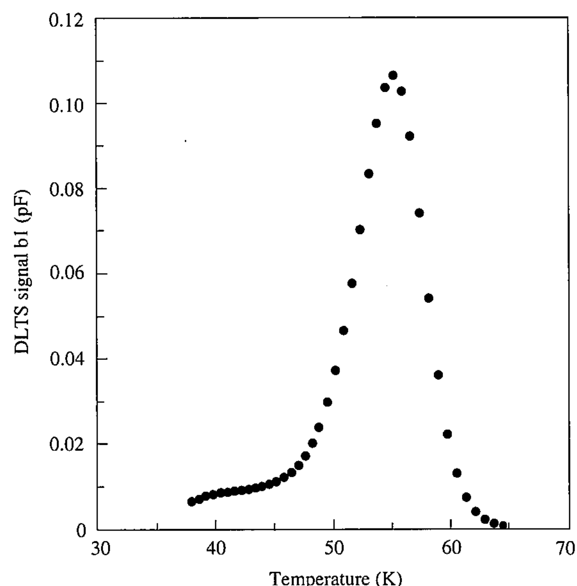


Fig. 11 DLTS signal of silicon wafer intentionally contaminated with iron

The DLTS method is available in very many variations, depending on the selection of the device structure to be examined (MOS, pn junction, or Schottky junction), the method of injecting majority carriers (electrical pulse or light), the range of voltage application (from accumulation to deep depletion), the measurement temperature, and the measurement time constant (window rate). It is a very powerful technique, if properly used. The features of DLTS are cited below.

DLTS can spectroscopically evaluate not only deep levels due to heavy-metal contamination, but also all trap levels in the band gap. The trap detection sensitivity is possible to a majority carrier concentration of 1/100,000 (to 1E-10/cm³ for 10-Ωcm p-type wafers). In addition to majority carrier traps, minority carrier traps can be evaluated by optical DLTS or pn junctions. The energy level and capture rate of each trap caused by multiple contamination can be spectroscopically isolated and evaluated. Evaluation can be made in a very narrow region of 0.1 mmφ. Schottky junctions can be evaluated without heat treatment because they only need to be formed by vacuum deposition. Some degree of isolation and evaluation can be achieved in the thickness direction by changing the depletion layer thickness with the voltage. The MOS interface states and the bulk traps can be evaluated separately.

Evaluation of the MOS interface states is considered to be very useful for evaluating contamination by nickel and other metals likely to concentrate at the MOS interface. Another advantage, especially in terms of gettering evaluation of epitaxial wafers with substrate oxygen precipitation increased for gettering and annealed wafers, is that the deep levels of defect-free surface layers can be precisely evaluated without being affected by the diffusion of minority carriers from the underlying substrate. The aforementioned MOS C-t method and pn junction leakage evaluation method are subject to the influence of the diffusion of minority carriers from the underlying substrate that constitutes gettering sites. They cannot precisely evaluate the generation lifetime τg (or leakage current) of the defect-free surface layer unless well structure formation or other measures are undertaken. DLTS measures the release process of majority carriers in such a short time region that they are not affected by the diffusion of minority carriers from the underlying substrate. As noted above,

DLTS is expected to become a very powerful evaluation tool in the development of next-generation wafers.

6. Conclusions

With the 0.13μm design rule generation in sight, the device manufacturing process is greatly changing. To meet the size reduction challenge, the gate oxide, for example, is reduced in thickness to the smallest possible degree and in metal contamination resistance as well. The device manufacturing process uses an increasing number of metal types, as evidenced by introduction of multi-layer interconnection, high-k materials, and low-k materials. Improvement in the gettering ability is demanded to ensure reliability. Gettering by oxygen precipitation in the device process cannot be expected because of process temperature reduction and epitaxial wafer introduction. Future silicon wafers will be required to provide a substrate with a high enough gettering ability at the time of shipment while assuring complete freedom from defects in the surface device region. Finer design rules and damascene interconnects will make it common to introduce chemical mechanical polishing (CMP) in later processes and impose wafer flatness requirements of increasing severity.

To develop the technology of producing such high-performance wafers with high productivity and high cost performance, it is necessary to develop new silicon wafers with flexible concepts. Epitaxial wafers produced from nitrogen-doped crystals, argon-annealed wafers, and ion-implanted epitaxial wafers combine defect-free surfaces with high gettering ability, and are considered as candidates for future high-functionality wafers.

References

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