Silicon Wafer Defect Engineering Synchronizing State of the Art Semiconductor Devices

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Abstract

Silicon semiconductor devices are showing remarkable advancement, and silicon wafers, the starting material of the devices, are facing demands for more fundamental advancement than the semiconductor devices. In the present situation where the devices face a paradigm shift from PC (personal computer) to IA (information appliance), high quality wafers having excellent cost performance are requested in order to cope with the trend of drastic chip shrinkage. It is through the "defect engineering" of grown-in defects of the wafers that the quality enhancement of the wafers was brought about in response to the latest advancement of the devices. Future requisites in the material structure of the silicon wafers are the total elimination of defects by point defect engineering both at the surface and the subsurface regions and the formation of high density defects by micro defect engineering to obtain high gettering capability in the wafer bulk. In the silicon wafer business, Nippon Steel has pursued enhancement of wafer quality and challenged defect engineering from the material science viewpoint. This paper outlines formation mechanisms of major grown-in defects, –void defects, dislocation cluster defects, and ring-OSFs– and then discusses the defect engineering measures against these defects as well as possible future trends, including the recently developed technique of nitrogen-doping.

1. Introduction

The effects of the technological innovations of silicon semiconductor devices deeply permeate not only our industries but also our daily lives. The intensity of this impact attests to the fact that the semiconductor is the greatest invention of this century. The silicon semiconductor devices have phenomenally increased in circuit density and speed, diminished in power consumption, and improved in functionality and reliability. There have been demands on silicon wafers, which are the starting materials of the silicon semiconductor devices, to make greater progress than silicon semiconductor devices.

As the road map of semiconductor device technology moves toward finer design rules, better surface flatness and larger wafer diameters, the markets where semiconductor devices are needed are structurally changing from personal computers (PCs) that have driven the semiconductor technology up to now to information appliances (IAs). In terms of devices, this structural change is equivalent from

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the age of data processing with microprocessors (MPs) to the age of large-capacity signal processing with digital signal processors (DSPs).

Subject to these market changes, the market trends are changing from growth based on increasing wafer consumption with increasing device units toward increasing cost performance with wafers through improving quality in response to chip shrink. In addition to the larger diameter wafers and epitaxial wafers that have traditionally been value-added sources, the wafer technology is demanded to provide still higher value added by enhancing the various quality properties of silicon wafers or crystals themselves.

The quality enhancement of silicon wafers in response to increasing device sophistication in recent years is achieved by "defect engineering", which means fabrication of required material structure by intentional control of crystal defects in the wafer. As far as Czochralski (CZ) silicon crystals are concerned, the 1980s could be considered to be the era of microdefect engineering represented by the control of oxygen precipitates in crystals originated in the research of Tan et al.[1] that regarded oxygen, an impurity up to then, as a useful element. The 1990s could be considered to be the era of point defect engineering represented by the control of crystal-originated pits (COPs) originated in the research of Ryuta et al.[2]

The quality enhancement initiative of the silicon wafer business of Nippon Steel Corporation (NSC) has consistently challenged the defect engineering of silicon wafers from a material science point of view since the inauguration of the silicon wafer business. In recent years, these efforts have borne fruit in the development of strong-impact products, including defect engineering[3] by nitrogen doping that can achieve both of the above-mentioned microdefect engineering and point defect engineering at the same time. This report discusses the actual situation of crystal defects as the key to the quality enhancement of latest CZ silicon crystals, and it introduces the future direction of CZ silicon crystal defect engineering.

2. Required Material Structures and Defect Engineering

The higher-quality material properties the silicon wafers are required to display with respect to finer design rules as they are fabricated in devices are higher gate oxide integrity (GOI) for excellent read and write characteristics, lower pn junction leakage and isolation leakage for excellent memory storage characteristics, and higher capabilities for removing the impurities of harmful heavy metal (gettering capability) in the low-temperature device fabrication processes (**Fig. 1**). To meet these material structure requirements, it is necessary to remove defects in the wafer surface and the wafer subsurface where the device is active and to form defects with gettering capability in the wafer bulk region. The defects referred to here include void defects, dislocation defects, stacking faults, and oxygen precipitates in crystals. These material structures must be accomplished by defect engineering on a mass production level with high controllability (independently, if possible), high reliability and low cost, and with the wafer diameter increase to 300 mm in view.

One quality enhancement feature of silicon wafers is not that there are specifications to be satisfied by some effective properties as indicators of high quality in the conventional material development hierarchy composed of the three stages: performance-property-structure, but that the structure itself directly produced by defect engineering, in other words, the number of defects in the silicon wafer, is an indicator of high quality for yield to satisfy the performance or electrical characteristics of the device and it is a common language in the silicon wafer market. For example, **Fig. 2** shows the relationship between the COP volume density of silicon wafers and the gate oxide dielectric breakdown yield of devices (proportion of MOS capacitor electrodes failing at a threshold current of 1 μA and voltage of 8 MV/cm). The breakdown yield is less than 10% for conventional crystals with a COP density of $10^6/cm^3$, but improves to more
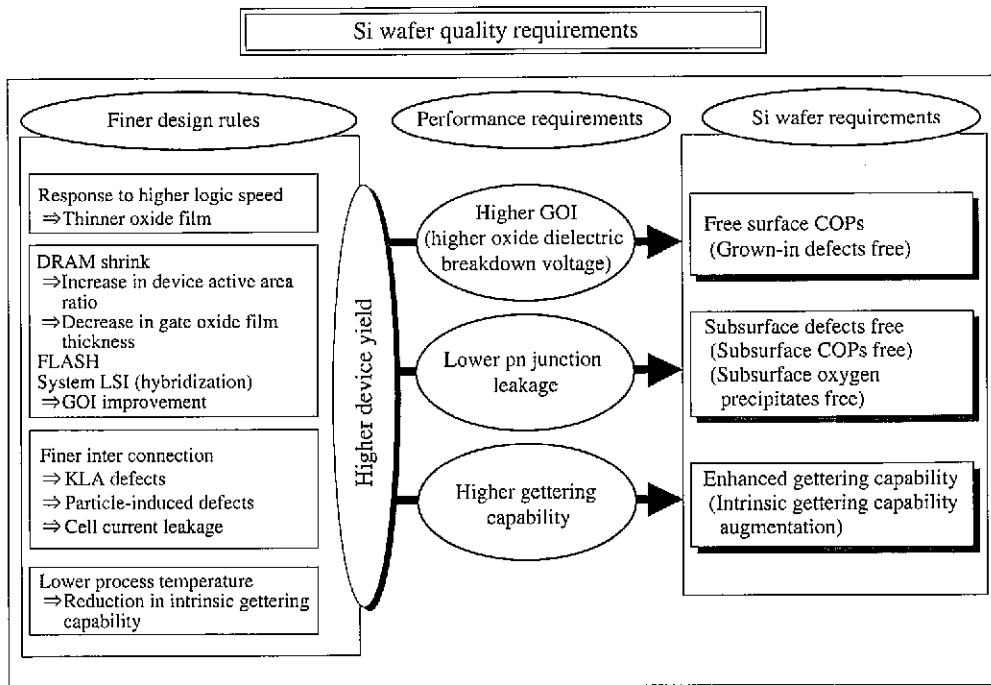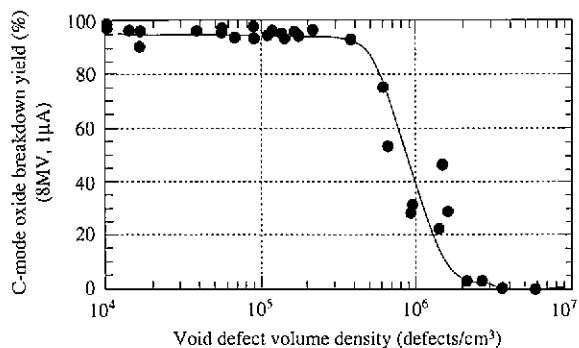

Fig. 1 Silicon wafer quality enhancement requirements

Fig. 2 Effect of volume density of void defects on oxide breakdown yield of silicon wafers (GOI yield at 8 MV/cm)

than 90% when the COP density is reduced to 10^5/cm^3 by quality enhancement with defect engineering.

3. Grown-in Defects in Silicon Crystals

3.1 Defect formation

Defects (void defects, dislocation defects, stacking faults, and oxygen precipitates) in silicon crystals are secondary defects called grown-in defects. Grown-in defects result from the phase transformation at a given agglomeration (nucleation) temperature of primary defects, or vacancies and interstitials, introduced at the solid-liquid interface during crystal growth. The agglomeration temperature of point defects varies with their type as shown in Fig. 3. It is affected by the amount of point defects introduced that depends on the conditions of the solid-liquid interface during crystal growth and by the crystal thermal history to which are subjected the point defects during crystal pulling. Specifically, the agglomeration temperature of point defects changes because their super-saturation degree changes with up-hill diffusion of vacancies from the crystal to the growth interface[3] or in-diffusion of interstitials from the growth interface into the crystal[4]. It is approximately 300 to 500°C lower than the solidification temperature.

3.2 Evaluation of grown-in defects

Void defects were initially detected by a wafer surface particle counter and were named COPs. The subsequent transmission electron microscopy (TEM) observation of electrical failures by the metal oxide semiconductor-electron beam induced current (MOS-EBIC) method[5] or copper decoration method[6] established a one-to-one correspondent observation between defects and electrical failures.

The authors mainly report here the density and size of grown-in defects evaluated by bright-field infrared laser interferometry (or with an oxygen precipitate profiler (OPP)). The optical system of the OPP

is shown in Fig. 4. An infrared laser beam is divided into two polarized beams and directed toward a silicon wafer. The transmitted beams are caused to interfere with each other to detect the phase difference that results from scattering proportional to the cube of the size of a defect[7]. NSC has associated on a one-to-one basis the signal intensity of various defects measured with the OPP with their actual size determined by TEM, and has achieved the practical method of evaluating grown-in defects with the OPP[8].

3.3 Void defects

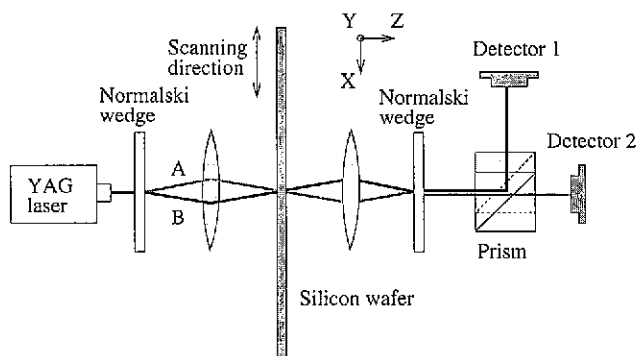Fig. 5 shows the one-to-one correspondent observation by TEM

Fig. 4 Principle of infrared laser interferometer (OPP) for evaluating grown-in defects in silicon crystal: Signal intensity changes with phase difference $\Delta\phi$ between beams A and B. Phase difference $\Delta\phi$ results from defects with different refractive index from matrix phase, such as precipitates or voids, or from dislocation clusters with anisotropic strain
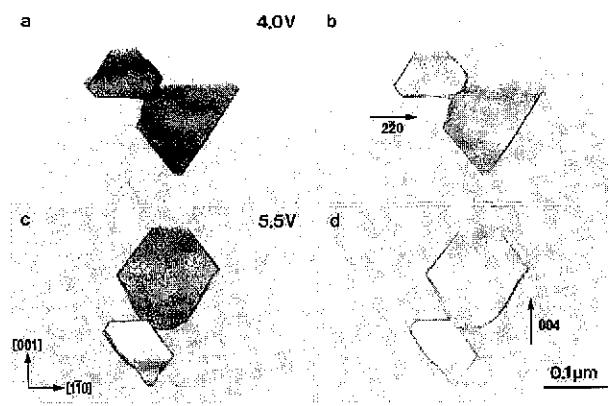
Fig. 5 TEM images of octahedral void defects detected with OPP in silicon crystal

Grown-in defects		Octahedral voids (D defects)	Dislocation cluster defects (A and B defects)	Oxygen precipitates
	Secondary defects			
Agglomeration onset temperature T*		T_m-T* - 330°C	T_m-T* - 450°C	T_m-T* - 400°C
Point defects		Vacancies	Interstitials	Interstitial oxygen + residual vacancies
	Primary defects			

T*
Agglomeration onset temperature
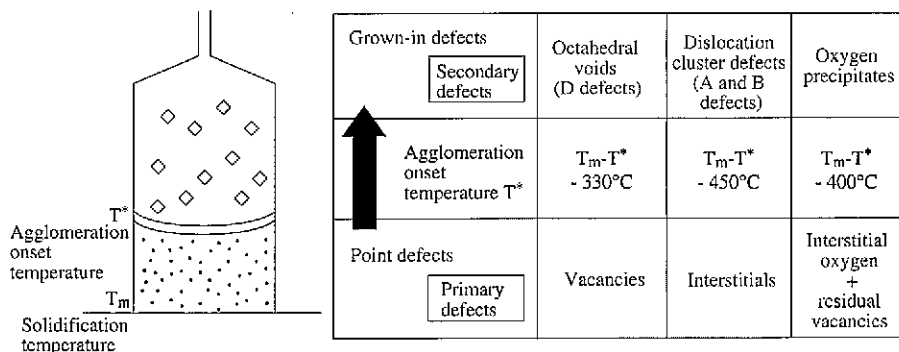
T_m
Solidification temperature

Fig. 3 Formation of grown-in defects from point defects in silicon crystal

of defects detected with the OPP in crystals grown at a conventional pulling rate or in what are called vacancy-dominant crystals. These voids affect the dielectric breakdown voltage of the gate oxide film as already described. They are octahedral negative crystal defects faceted with {111} planes at a volume density of up to 10^6/cm^3 in the wafer and ranging 0.1 to 0.5 μm in size. A thin oxide film is formed on the inside of the void defects. Observation of Fresnel fringes made it clear that these defects are really cavities. Many of the void defects exist in pairs and accompanying truncated facets {100}. The discovery of such void defects and the appearance of their effect on devices have been the major driving forces behind the quality enhancements of silicon wafers in recent years. It is interesting to note that more than 20 years before this identification of voids as octahedral defects, Voronkov theoretically predicted even their octahedral morphology as vacancy type defects[9].

The authors investigated with pulling-halted crystal experiments to clarify the agglomeration reaction of vacancies[10] as primary defects[11]. During their pulling, crystals were held for a long period of time according to a given temperature history to reveal the defect reactions occurring in each holding temperature region. **Fig. 6 (a)** shows the cumulative volume density of void defects detected in crystals held for 60 minutes during pulling and above a given signal intensity or size in relation to the holding temperature. The crystal portions held in the temperature region of 1,070 to 1,100°C alone are decreased in the cumulative volume density of void defects showing a signal intensity of more than 0.2 V and corresponding to the total defect volume density, and are increased in the cumulative vol-

ume density of voids with a signal intensity of more than 10 V.

The measured gate oxide film dielectric breakdown yield of the same crystal portions is shown in **Fig. 6 (b)**. It is evident that in the holding temperature region where the total defect density is reduced as noted above, the MOS capacitor electrodes that have a failure ratio in an electric field with a strength of 8 MV/cm or less, are decreased and improved in dielectric breakdown voltage (Also see to Fig. 2). This result shows that the formation and growth of void defects and the attendant reduction in the total defect density occur in an extremely narrow temperature region.

Fig. 7 shows the void defect size distributions measured with the OPP by changing the holding time in the above void defect nucleation temperature region, in order to understand the formation and growth of void defects in greater detail. Changing the holding time from 7 min to 100 min annihilated smaller defects, formed larger defects, and shifted the average defect size to the higher end of the size distribution. **Fig. 8** shows the changes in the size, density, and cumulative total volume of defects formed in silicon crystals held in the temperature region of 1,070 to 1,100°C. Increasing the holding time increased the defect size and decreased the defect volume density, but kept the total defect volume approximately constant. The phenomenon, known as Ostwald ripening, is considered to have occurred. When the concentration of supersaturated vacancies that contributed to the formation of void defects is estimated from the total defect volume by assuming that one vacancy has a volume of about 10^{-2} nm^3, it is about 10^{13} to 10^{14}/cm^3. When defect growth in direct proportion to the 1/2-th power of the time in Ostwald ripening is considered in the light of the Lifshitz-Wagner law, it is presumed that the growth of void defects is controlled by the reaction rate when vacancies agglomerate at the defect interface.

3.4 Dislocation cluster defects

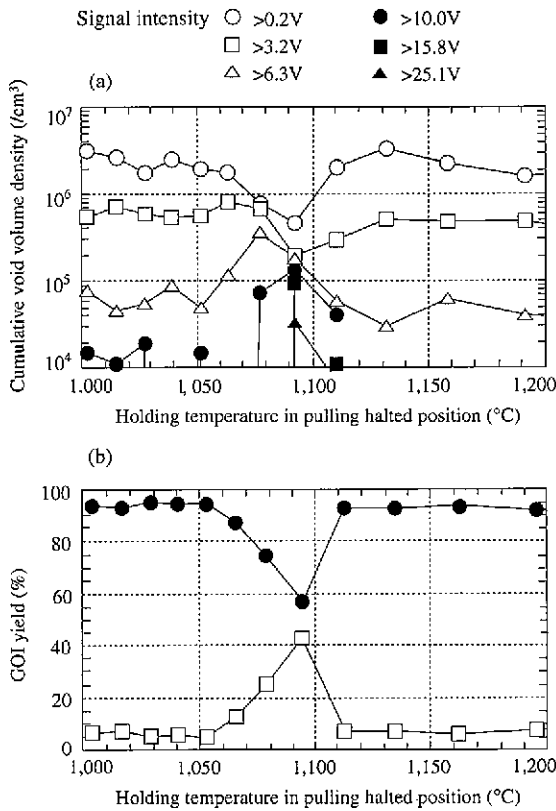When the crystal pulling rate is reduced from the rate at which

Fig. 6 (a) Cumulative volume density of voids larger than a given size in crystals whose pulling was halted for 60 min, and (b) GOI yield at 8 MV/cm (b). Horizontal axis indicates holding temperature in pulling halted position
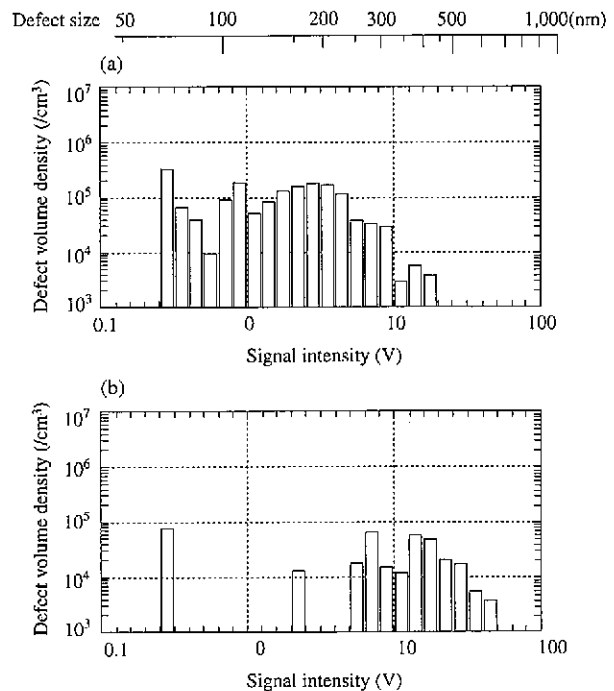

Fig. 7 Histograms of grown-in defect density signals measured with OPP in crystals held for 7 min (a) and 100 min (b) at void nucleation temperature of 1,070 to 1,100°C during pulling
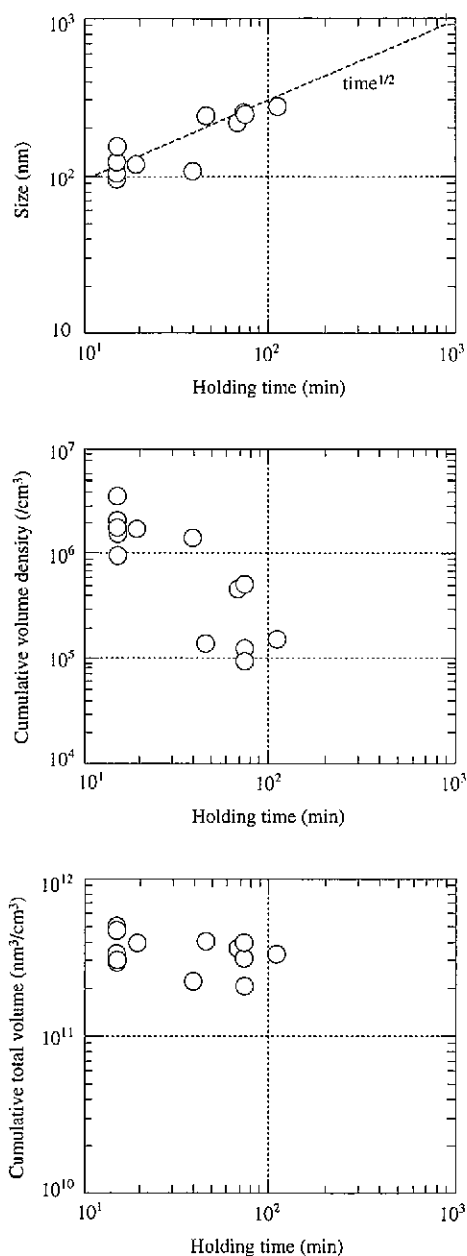
Fig. 8 Size, cumulative volume density, and cumulative total volume of defects in crystals held at void defect nucleation temperature of 1,070 to 1,100°C during pulling. Horizontal axis indicates holding time
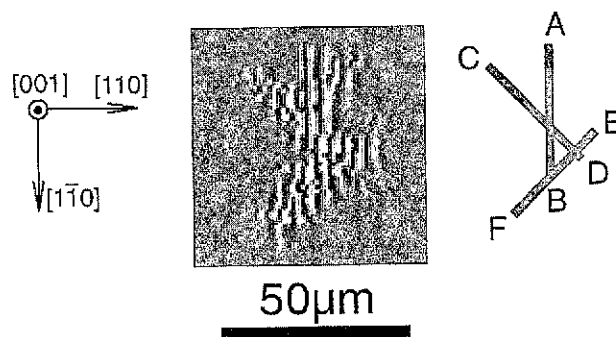

Fig. 9 Image of typical dislocation cluster measured with OPP in crystal pulled at low rate of 0.4 mm/min: Segments A, B, and C are extended in [110], [10$\bar{1}$], and [011], respectively

void defects form, the dominant type of point defect changes from vacancies to interstitials, with the result that the main type of grown-in defects changes from void defects to dislocation cluster defects[12]. An image of a crystal grown at a pulling rate of 0.4 mm/min and observed with the OPP is shown in Fig. 9. The volume density of defects is up to about 10^3/cm^3. The defects are dislocation clusters composed of segments ranging from 30 to 50 μm in size. The respective segments are elongated in particular crystal orientations. In Fig. 9, the segments AB, CD, and EF are three-dimensionally elongated in the orientations [110], [10$\bar{1}$], and [011], respectively. For the TEM observation of the defects, a specimen was prepared along the segment AB in Fig. 10 (a). The results are shown in Fig. 10 (b).

A bundle of perfect dislocations is observed elongated in the orientation [110], and stacking faults are recognized in the region enclosed with a square box in Fig. 10 (b). The ends of perfect dislocations are in contact with the stacking faults.

When the Burgers vectors of the stacking faults and perfect dislocations were examined, a/3 [111] of the Frank partial dislocations and a/2 [10$\bar{1}$] and a/2 [110] were identified about the stacking fault as indicated by A, B, and C, respectively, in Fig. 11. Contrast observation found that the stacking faults were of the extrinsic type with interstitials agglomerated in the lattice plane. A careful observation of the above-mentioned interface between the stacking fault and perfect dislocation end confirmed the presence of a micro-defect regarded as an oxygen precipitate (indicated by the arrow in Fig. 12).

It is thought that interstitials supersaturated during crystal growth agglomerated to form a stacking fault and that a perfect dislocation of lower energy was formed from the stacking fault by the reaction between a Frank partial dislocation and a Shockley partial dislocation. The concentration of interstitials forming the stacking faults is estimated at up to 10^{13}/cm^3. Interestingly, this concentration is of approximately the same order as that of the concentration of vacancies forming void defects.

Crystals grown at this low pulling rate are free from void defects and exhibit relatively good gate oxide integrity, but are practically disadvantageous in low pn junction leakage[13]. The formation, growth, size, density, and primary point defects of void defects and dislocation cluster defects are summarized in Table 1.

3.5 Ring-OSFs

Before the above-mentioned void defects and dislocation cluster defects were recognized as major defects that govern the electrical characteristics of wafers, secondary defects in CZ silicon crystals had been mainly oxidation-induced stacking faults (OSFs) formed by the heat treatment of wafers and oxygen precipitates. OSFs are OSFs induced by mechanical strain or impurities and ring-OSFs induced by point defects described below.

The ring-OSF occurs as a ring in the wafer plane after heat treatment as shown in Fig. 13[14]. The ring OSF is positioned just like a marker at the boundary between a void and a dislocation cluster defect (accurately, slightly on the vacancy-dominant side of the intrinsic boundary). In the in-plane distribution of a wafer grown under a conventional pulling history, voids are dominant inside of the ring-OSF, and dislocation cluster defects are practically dominant outside of the ring-OSF. It is known that the ring-OSF shrinks toward the center of the wafer as the pulling rate is decreased[15] and that
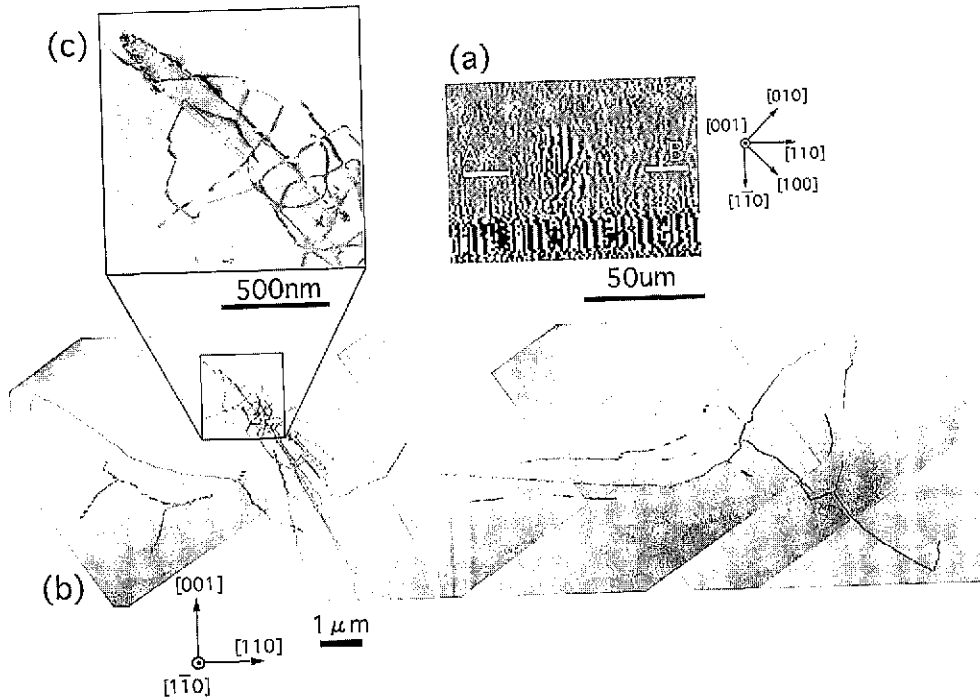
Fig. 10 OPP detection image (a), bright-field TEM image (b), and stacking fault initiation point (c) (enlarged view of region enclosed with square box in (b)) of dislocation cluster defect. Specimen for TEM observation was machined along line AB in (a)
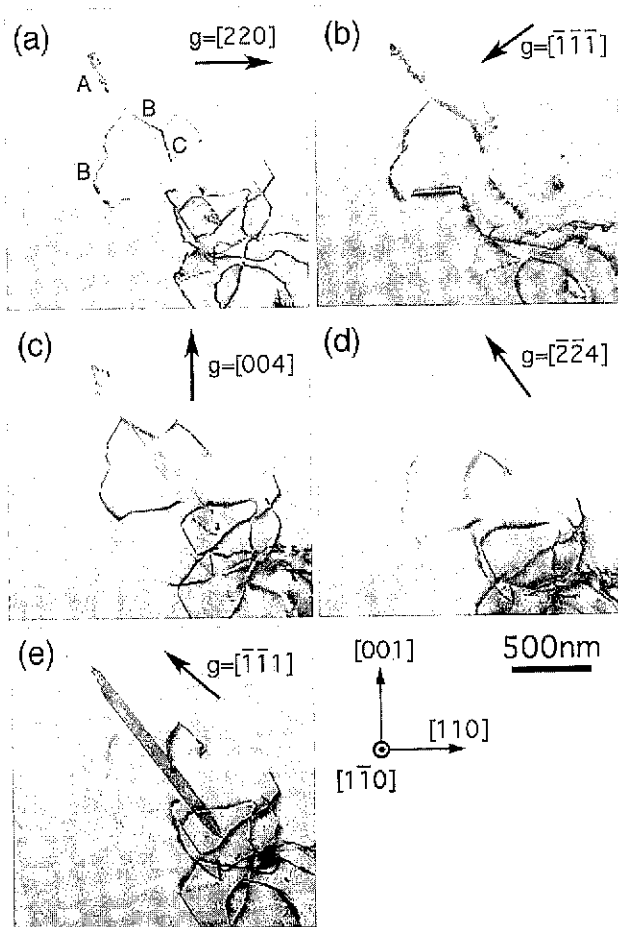

Fig. 11 Bright-field TEM images of stacking fault (A) and perfect dislocation (B, C) (g: diffraction vector)
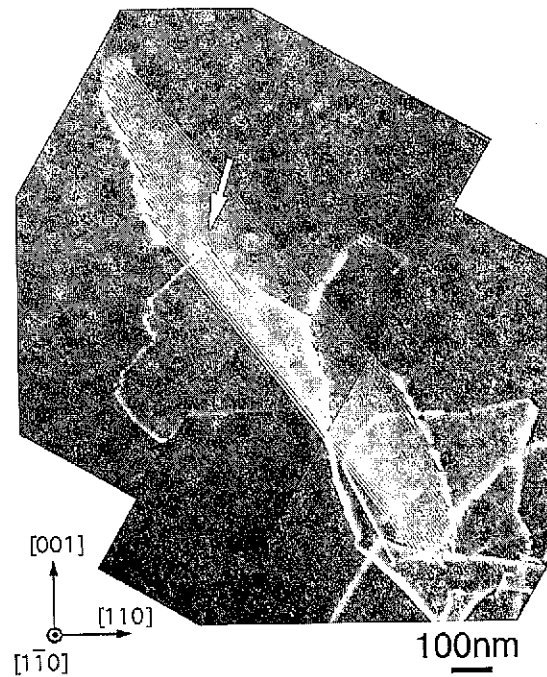

Fig. 12 Micro defect at interface between dislocation and stacking fault: Indicated by white arrow

oxygen precipitates are present at the center of the OSF formed after heat treatment.

Fig. 14 shows the results of a pulling-halted experiment conducted to investigate the behavior of ring-OSFs. When the crystal was held for 7 min, the ring-OSF was already starting to shrink toward the center of the wafer. When the crystal was held for 100 min, the ring

Table 1 Features of void defects and dislocation cluster defects in silicon crystals

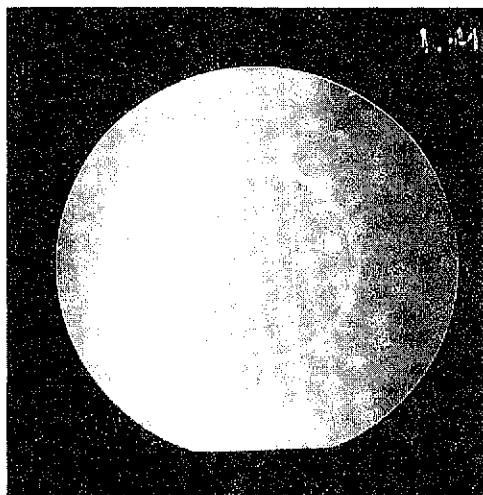| Feature	Defect	Dislocation cluster defect
Constituent point defect	Vacancy	Interstitial
Defect morphology	Truncated octahedron Facet{111}/{100}	Perfect dislocation of <100> direction segment and stacking fault
Defect size	100 to 300 nm	~ 50 μm
Defect density	~ 10^6/cm^3	~ 10^3/cm^3
Defect formation	Rapid nucleation and growth due to vacancy agglomeration (formation promoted by oxygen)	Formation of extrinsic stacking fault due to interstitial agglomeration
Onset	~ 1,080°C	~ 1,000°C
Growth	Ostwald ripening (constant total volume, increasing size, and decreasing density) Proportional to 1/2-th power of time	Initiation of perfect dislocation from stacking fault (or micro oxygen precipitate at interface)
Total number of point defects	10^{13} to 10^{14}/cm^3	10^{13} to 10^{14}/cm
Affected electrical property	B mode gate oxide dielectric breakdown voltage	Pn junction leakage

Fig. 13 Ring-OSF distribution in plane of wafer in silicon crystal (X-ray topographic image after 1,100°C oxidation heat treatment)

was completely closed, and a dislocation cluster defect-dominant region was formed near the interface. This phenomenon shows that in a crystal where vacancies were initially dominant, up-hill diffusion of vacancies (V) from the crystal to the growth interface[3] or in-diffusion of interstitials (I) from the growth interface to the crystal[4] as already noted changed the vacancy dominance to the interstitial dominance.

To investigate the defect distribution near the ring-OSF in greater detail, a crystal was stopped for 100 min and analyzed in the as-grown condition for the secondary defect distribution in the crystal pulling direction. The results are shown in **Fig. 15** (the crystal pulling direction is from right to left in the page). In the region where the ring-OSF is closed, dislocation cluster defects exist with a density of up to 10^3/cm^3 and decrease in size as they approach the ring-OSF. This is accompanied by a concomitant reduction in the calculated cumulative concentration of contributing interstitials. A bit inside of the ring-OSF at the leftmost end in Fig. 15, voids were confirmed

with a density of up to 10^6/cm^3. Slightly outside of the ring-OSF, there exists a localized, central region where both void and dislocation cluster defects are not existent.

Just in the position where a ring-OSF would form after heat treatment, a defect that wa neither a void nor a dislocation cluster defect was detected with a density of up to 10^6/cm^3. This defect was evaluated. It was found to be a stacking fault as shown in **Fig. 16 (a)**, and the presence of a nucleus, speculated to be an oxygen precipitate, at its center was confirmed as shown in **Fig. 16 (b)**. This is the first experimental fact that in the ring-OSF after heat treatment, there already exists an oxygen precipitate as its nucleus in the as-grown state.

3.6 Formation of point defects and grown-in defects

The formation of grown-in defects discussed up to now is considered from the standpoint of the distribution of point defects in crystals. **Fig. 17** shows the relationship between the initial radial distribution of point defect concentration and the residual point defect concentration after phase transformation of point defects to secondary defects, and presents the in-plane grown-in defect distribution reflecting these results. The initial radial distribution of point defect concentration is determined by the pulling parameter V/G or ratio of the crystal pulling rate V (more accurately, the crystal growth rate) to the temperature gradient G in the crystal length direction at the solid-liquid interface[4]. The dominant point defect species is vacancies when the V/G ratio is higher than the critical value and is interstitials when the V/G ratio is lower than the critical value. In Fig. 17, C_v is the vacancy concentration, and C_i is the interstitial concentration. The pulling rate V is uniform in the plane. As far as the in-plane distribution of G is concerned, G is lower at the edge of the wafer than at the center of the wafer, so that V/G is higher at the center of the wafer than at the edge of the wafer. As shown in Fig. 17, both C_v and C_i become zero at the critical V/G ratio. The critical V/G ratio is known to change also with the addition of boron and other impurities to silicon crystals.

The crystal center with a highly-supersaturated effective vacancy concentration C_v transforms to a void at the aforementioned void nucleation temperature. As the super-saturation degree decreases, the nucleation temperature shifts toward the low end of the nucleation temperature range. In the vicinity of 1,000°C, the super-saturation
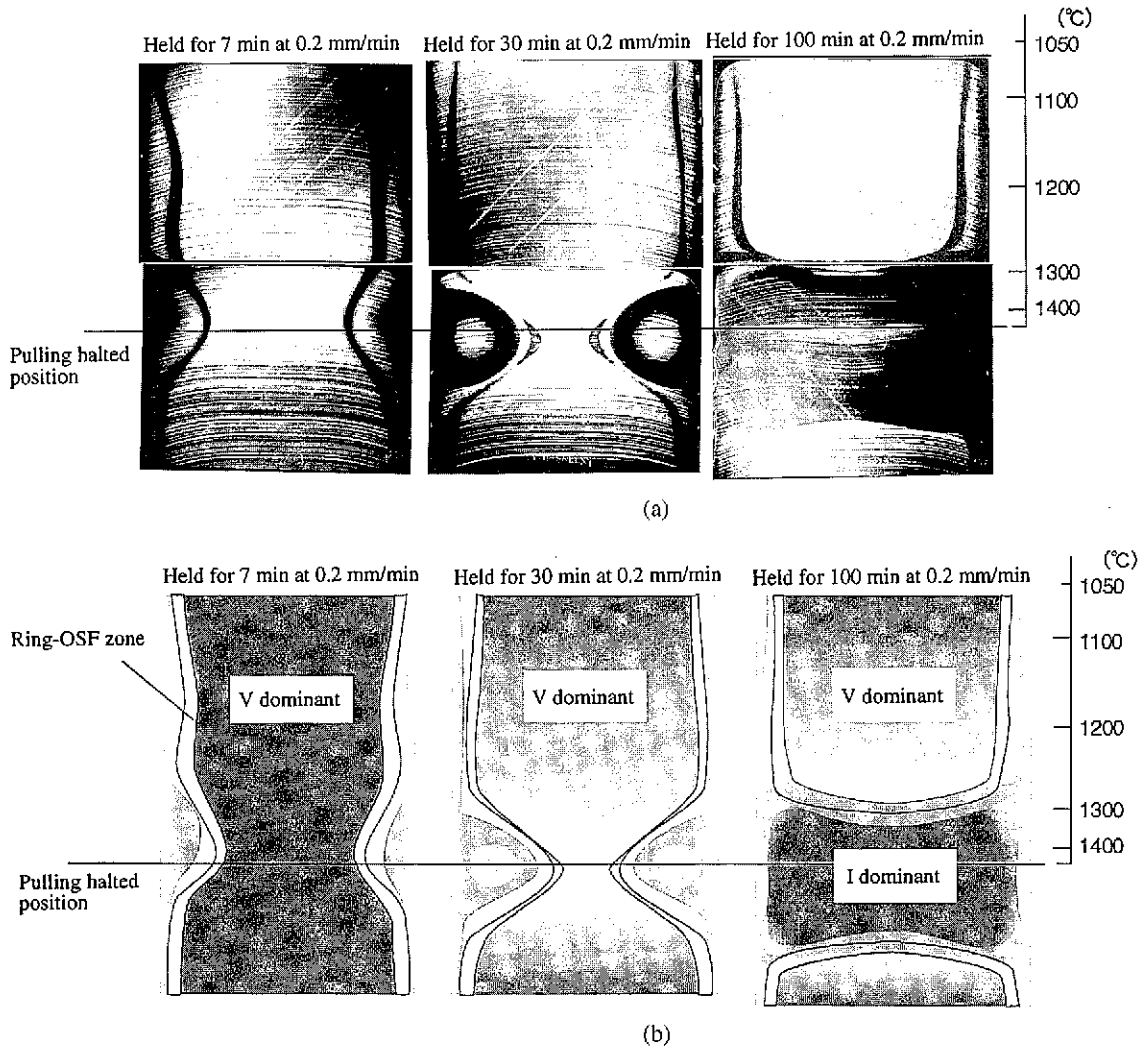
Heat treatment: 800°C, 4 hrs + 1,000°C, 16 hrs

(a)

(b)

Fig. 14 (a) Change in ring-OSF distribution on vertical section of crystal in experiment in which pulling of silicon crystal was halted for 7 to 100 min (X-ray topographic images after heat treatment at 800°C for 4 hrs and at 1,100°C for 16 hrs). (b) Dominant point defect species corresponding to change in ring-OSF distribution

degree is so low that residual vacancies that did not transform to voids combine with oxygen atoms to form VO_2 complexes and stop their agglomeration to voids. Here, the ring peak distribution of VO_2 complexes is considered to remain in the plane, and ultra-fine oxygen precipitates are considered to form with a volume density of up to $10^6/cm^3$ in the as-grown condition and to nucleate the ring-OSF after heat treatment.

At both sides of the ring distribution where ultra-fine oxygen precipitates are formed, there are still residual vacancies. These residual vacancies are considered to nucleate oxygen clusters with a volume density of up to $10^9/cm^3$ in the temperature region of 650 to 700°C[16]. As a result of this series of reactions, the grown-in defects are distributed in a ring pattern sequentially from the center of the silicon crystal as follows: void defect zone, residual vacancy zone (inside of the ring-OSF), ultra-fine oxygen precipitate zone (ring-OSF zone), residual vacancy zone (outside of the ring-OSF), residual interstitial zone, and dislocation cluster defect zone. The residual vacancy zone (outside of the ring-OSF) and residual interstitial zone are called together as defect-free neutral zones.

4. Issues and Future Direction of Defect Engineering

This section discusses defect engineering for rendering the wafer surface and device-active subsurface free from defects as demanded by devices and for accomplishing the high-density formation of defects for gettering in the wafer bulk. Among the possible defect engineering methods for meeting these contradicting material structure requirements are crystal thermal history control to directly change grown-in defects during crystal growth, high-temperature wafer anneal to change grown-in defects after wafer fabrication, and epitaxial wafer fabrication to form a fresh defect-free crystal layer on the wafer.

4.1 Thermal history control during crystal growth

Thermal history control for defect denudation during crystal growth may cover two main types of crystals. One type is a low-COP crystal designed to keep the void density below a given value, and the other is a neutral zone crystal designed for perfect defect denudation.

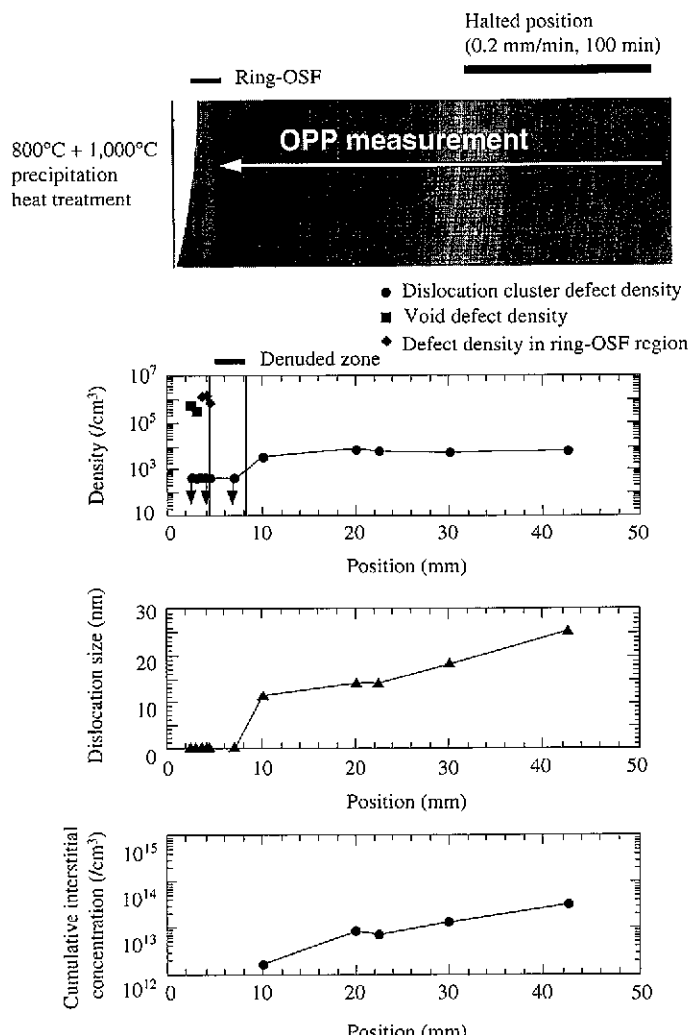Crystal thermal history control for low-COP crystals can be con-

Fig. 15 Grown-in defect distribution near ring-OSF zone (crystal halted for 100 min): Dislocation cluster defects, void defects, and defects in R-OSF region
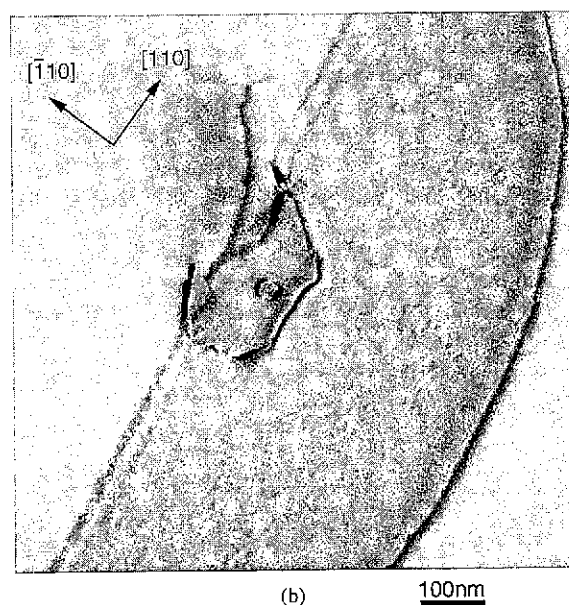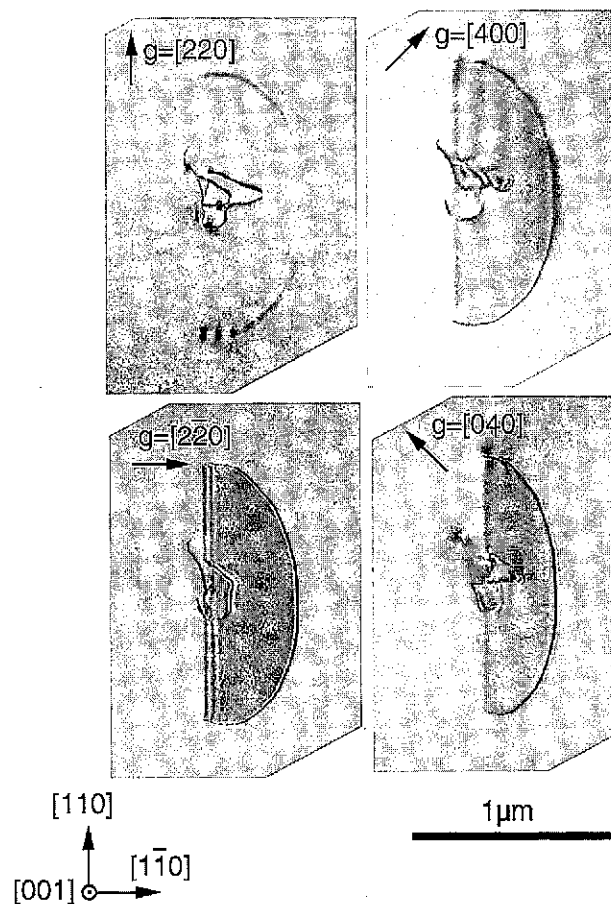

Fig. 16 (a) Stacking fault and its nucleus observed in "as-grown" condition in ring-OSF region, and (b) enlarged view of nucleus (probably oxygen precipitate)

sidered in two steps as shown in **Fig. 18**. The first step consists of reduction in the vacancy supersaturated concentration itself to the void nucleation temperature (T*) and of control to the defect size and density demanded by the devices at the void nucleation temperature. The vacancy concentration may be reduced by the combination of up-hill diffusion of vacancies to the solid-liquid interface by use of the temperature dependence of the vacancy saturated concentration gradient near the solid-liquid interface with out-diffusion of vacancies to the periphery of the crystal by use of the concentration gradient.

Fig. 19 shows the density and size of voids achieved by the low-COP control method. Conventional crystals are used as starting materials, and the vacancy concentration is kept constant. Crystal A was rapidly cooled at the void nucleation temperature. The voids formed in crystal A are decreased in size and increased in density. Crystal B was slowly cooled at the void nucleation temperature. The voids formed in crystal B are increased in size and decreased in density. Generally, crystal B evaluates better than crystal A in gate oxide film dielectric breakdown voltage, so it could be said that it is more effective in reducing the void density than the void size if design rules are below certain levels. Crystal C was grown by decreasing the vacancy concentration but not changing the cooling rate. The voids are

decreased in size, but are slightly increased in density. Slower cooling of crystals D and E increases the void size and decreases the void density in that order. These low-COP crystals are limited in their
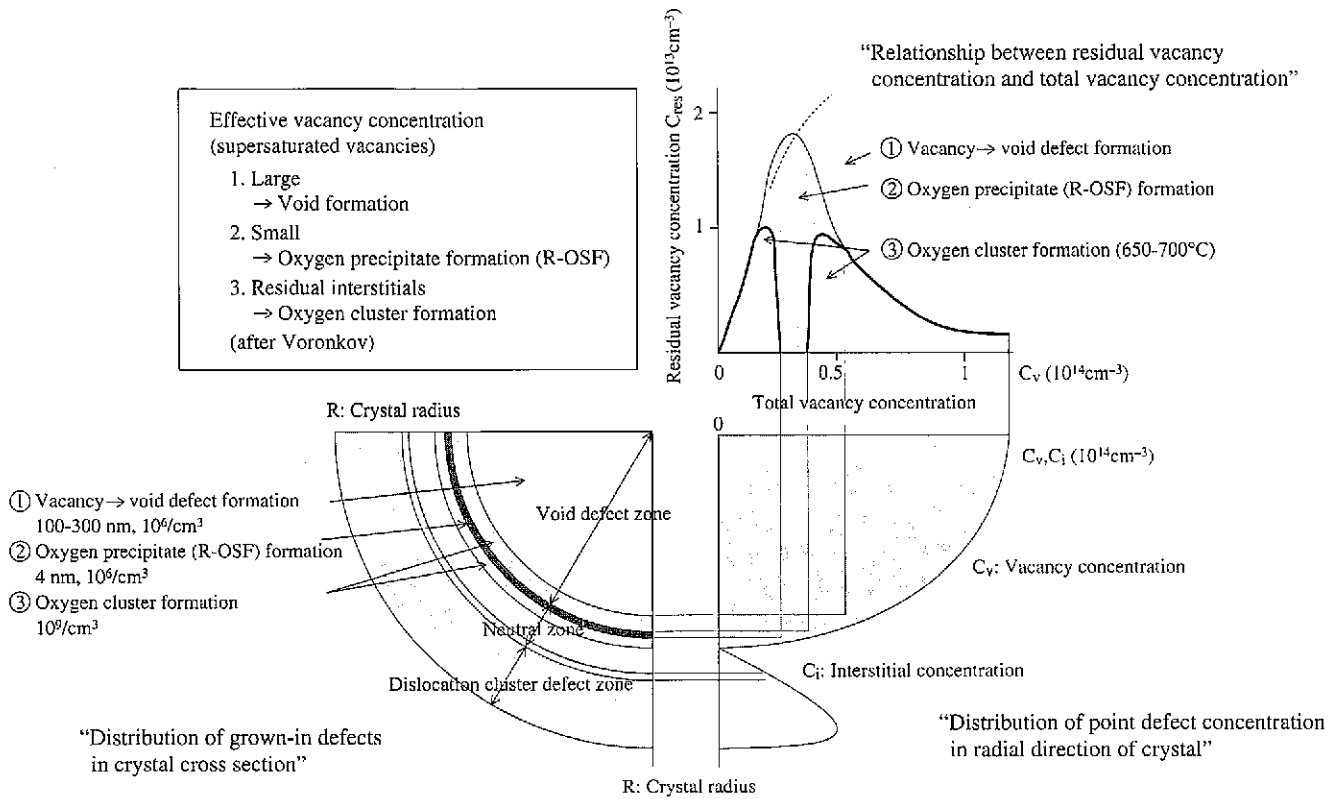
Fig. 17 Point defect distribution and formation of grown-in defects in silicon crystal

application to advanced devices because they are pulled at lower rates and because their void defects cannot be completely eliminated.

The neutral zone crystal is fabricated by such a method that the neutral zone that falls between the void zone and the dislocation cluster zone as already discussed is enlarged throughout the plane of the crystal[17] and is extended along the length of the crystal as well. This method calls for the in-plane V/G ratio to be controlled uniformly and accurately. Because the neutral zone crystal is sometimes affected by slight changes in the thermal conditions of the crystal growing crucible and in convection of the silicon melt, for example, its pulling rate must be reduced in such a case. This makes it difficult to use neural zone crystals for larger wafers. Neutral zone crystals also consist of vacancy and interstitial zones as already described. During device heat treatment, the vacancy zone has active oxygen precipitation due to the presence of oxygen clusters, but the interstitial zone has a lower capability to precipitate oxygen. This variation in

gettering capability with the in-plane oxygen precipitation is another problem with the neutral zone crystals.

4.2 High-temperature wafer anneal

The high-temperature wafer annealing method consists of growing a void defect region crystal in the crystal stage and annealing the wafer at a high temperature of 1,200°C in the wafer stage to annihilate surface and subsurface void defects. Wafers high-temperature annealed in a hydrogen ambient are developed and commercialized[18]. Hydrogen anneal was initially touted to have a unique effect of reducing the oxide layer formed in the inside walls of voids. Recently, annealing in a hydrogen ambient was reported to be as effective as annealing in an argon ambient[19, 20]. To provide a defect-free zone thickness from the surface, annealing at higher temperatures (e.g., 1,300°C)[21] is employed, or smaller voids are introduced into the starting crystal. Rapid thermal annealing (RTA) is also reported to be effective in this respect[22].

The recent technological trends of annealed wafers are to change from a void defect-free surface to a void defect-free subsurface as device active region and to assure the stable precipitation of oxygen with a high density in the bulk region for gettering in a low-temperature process. When a high density of bulk oxygen precipitates is required, it is necessary to increase the bulk oxygen concentration, with the result that oxygen reprecipitation occurs near the void defect-free subsurface. Another challenge is the accomplishment of high throughput and high yield without impurity contamination by high-temperature annealing to lower the cost and to adapt to larger wafers.

4.3 Epitaxial wafers

Epitaxial wafers were considered to have a completely defect-free subsurface because they form new epitaxial layers. Recently, it
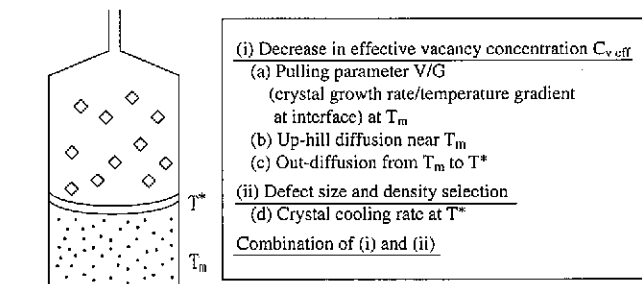

Fig. 18 Schematic of void defect control by thermal history control in crystal
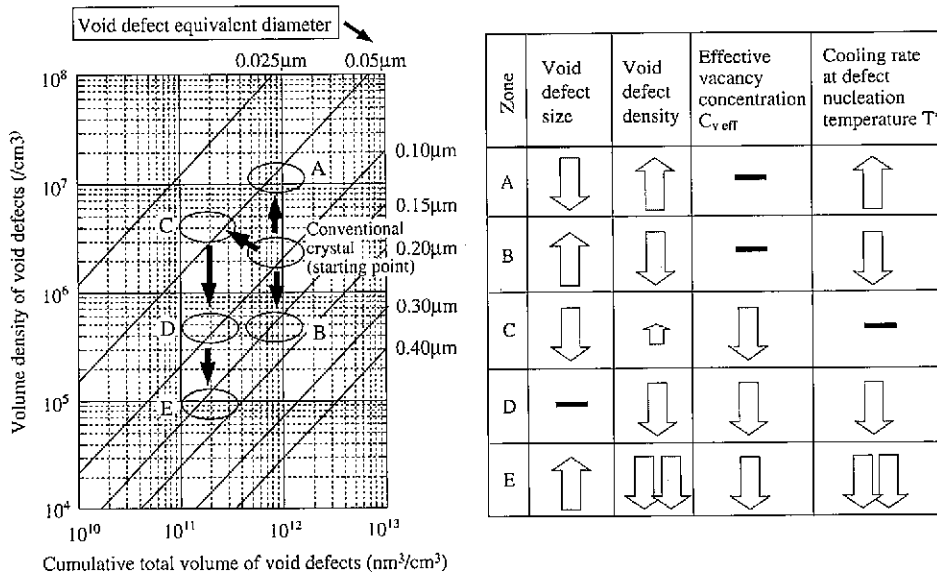
Fig. 19 Schematic showing relationship among crystal cooling rate, vacancy concentration, defect size, and defect density at void nucleation temperature region for low-void defect engineering

was reported that stacking faults are formed in epitaxial layers due to foreign matter and that fine void defects are formed even during epitaxial growth from the gas phase in the same way as noted for conventional CZ crystals grown from the liquid phase, despite the difference in the supersaturation degree[23]. Accelerated oxide precipitation[24] is reported to result from the return of oxygen back into the epitaxial layer. In addition to these low-density defects, epitaxial wafers also involve the future problems of providing substrate wafers with a satisfactory gettering capability by high-density and stable oxygen precipitation in response to the low-temperature device process; pulling substrate crystals at high rate, and reducing cost by increasing the throughput of the epitaxial process. Especially concerning oxygen precipitation, rapid heat treatment in the epitaxial process annihilates ordinary oxygen precipitation nuclei, so that preliminary heat treatment (near 800°C, for example)[25] becomes necessary for oxygen precipitate nucleation before epitaxial growth.

4.4 Future direction

Issues with defect engineering are summarized in **Table 2**. The diversification of high-quality wafers is taking place, including low-COP wafers and neutral zone wafers by thermal history control, high-temperature annealed wafers, and epitaxial wafers. To meet the contradictory defect engineering requirements of more complete freedom from defects in the subsurface and provision of high-density oxygen precipitates in the bulk, defect engineering capable of independently controlling the subsurface defects and the bulk oxygen precipitates will become inevitably advantageous.

Defect engineering by nitrogen doping[26], recently developed by the authors, is a method whereby point defect engineering to refine or annihilate voids and microdefect engineering to increase the density of oxygen precipitates can be both controlled in a favorable direction. More specifically, nitrogen doping changes the morphology of void defects from octahedral to platelet triclinic, and reduces their

Table 2 Issues of silicon wafer defect engineering

Directions		Issues
Thermal history controlled CZ	Low-COP crystal	· Not COP free · Low productivity · Larger wafer diameter
	Neutral zone crystal	· Low productivity and low crystal yield · Oxygen precipitation characteristic (difference in precipitation with different point defect species) · Perfection of neutral zone · Larger wafer diameter
High-temperature annealed wafer		· Perfection of COP free and precipitate-free layer (DZ layer) · Higher and confined oxygen precipitate density · Contamination · Larger wafer diameter
Epitaxial wafer		· Stable oxygen precipitation · Perfection of epitaxial layer (low-density defects, copy of defects from substrate) · Defect formation by oxygen climbing back into epitaxial layer · Cost
Intrinsic gettering capability		· Response to low-temperature process · Response to low-diffusion rate elements

size. It forms high-density platelet oxygen precipitates in as-grown crystals. Increasing the amount of nitrogen doping reduces further the size of void defects and eventually annihilates the void defects, and increases the density of grown-in oxygen precipitates. Since the oxygen precipitates exist in the as-grown state, their change in the subsequent process is growth (or annihilation) controlled by the simple diffusion of oxygen and is high in controllability. Among defect engineering applications in response to the advancement of devices by nitrogen doping are high-temperature annealed wafers, epitaxial wafers, and neutral zone wafers. The details are introduced in the respective papers in this special issue. The specific wafers are outlined below.

First, nitrogen doping reduces the size of void defects and forms as-grown high-density oxygen precipitates in high-temperature annealed wafers. In the next high-temperature annealing process in a non-oxidizing ambient like argon, the void defects and oxygen precipitates are efficiently annihilated in the subsurface oxygen-undersaturated region, and the oxygen precipitates grow in the bulk oxygen-supersaturated region. As a result, defect annihilation occurs more completely in the defect-free subsurface layer than in conventional wafers. A defect-free subsurface layer of ideally sufficient thickness can be produced by a relatively low-temperature anneal, and oxygen precipitates with a high enough density for gettering are already formed in the bulk in the wafer shipment stage. Electrical properties, such as gate oxide film dielectric breakdown voltage in the subsurface, are much higher than those of conventional annealed wafers and are comparable to those of epitaxial wafers. A powerful gettering capability is confirmed by simulation with intentional contamination in the low-temperature device process. It is also clarified that nitrogen doping has the secondary effects of increasing the mechanical strength and slip resistance of wafers.

Next, nitrogen doping is also effective on epitaxial wafers. In the case of a conventional crystal, epitaxial layer deposition and heat treatment annihilate oxygen precipitation nuclei in the substrate. An additional heat treatment is required for nucleation of oxygen precipitates before epitaxial layer deposition. Since grown-in oxygen precipitates are formed by nitrogen doping of the substrate, epitaxial layer deposition without pre-heat treatment produces precipitated oxygen at a high enough density for a high gettering capability. These oxygen precipitates formed by nitrogen doping are confirmed to act as more effective relaxation-type gettering centers than conventional oxygen precipitates.

The third and last is the neutral zone crystal. Nitrogen doping changes the grown-in crystal defect distribution in such a way that the decrease in the effective point defect supersaturated concentration by nitrogen expands the OSF defect zone as well as the neutral zone. The expansion of the neutral zone can be utilized to expand the controllable range of the neutral zone crystal. The other problems discussed above still call for future developments.

5. Conclusions

Defect engineering of silicon wafers in response to the paradigm shifts in the markets where semiconductor devices become commodities will have to be able to apply similarly to 300-mm silicon wafers, guarantee fast crystal pulling, and control both point defects and micro defects with industrial reliability and stability. Solutions for quality enhancement will initially diversify, but will eventually converge to higher-cost performance wafers featuring bulk manufacture at very low cost and provided with a necessary surface structure composed of a single layer (or multiple layers if required) (e.g., nitrogen-doped argon-annealed wafers and nitrogen-doped epitaxial wafers, both developed by NSC). Defect engineering adapted to the sophistication of devices in the future silicon wafer business will select the structures necessary in the evolution of total solution with the device processes.

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