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SIMOX Wafers
(Silicon wafers with a thin superficial silicon film separated from the body by implanted oxygen)

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Abstract:

The quality of low-dose SIMOX wafers has been markedly improved and are expected to be promising materials for low-power CMOS devices. This has been accomplished by the optimization of oxygen ion implantation conditions and annealing conditions, introduction of internal thermal oxidation technology, control of metal contamination and dust generation in the oxygen ion implanter, and prevention of slipping in the annealing furnaces. Their properties, including film thickness uniformity, crystallinity, contamination, buried oxide dielectric strength, and gate oxide integrity have consequently improved to such high levels that they are applicable to LSIs. This feasibility has been demonstrated through the trial fabrication by a user of ULSIs from low-dose SIMOX wafers. The major problems to be solved are the reduction in the pipe density of the buried oxide and the reduction in the manufacturing cost.

1. Introduction

As the spread of electronic information processing in recent years into our daily lives has been accelerated by the increasing popularity of the Internet and multimedia, the need for large-scale integration circuits (LSIs) of the low power consumption type has mounted. High-speed processing of large volumes of data, such as moving pictures, calls for LSIs of higher element density and drive frequency. The concomitant increase in power consumption, however, is likely to cause the LSIs to exceed their heat dissipation limits. Here arises the demand for low-power LSIs. The increasing need for data processing and communication with personal digital assistants (PDAs) also translates into a demand for low-voltage and low-power LSIs. The power consumption of LSIs is reduced in all stages of system design, circuit design, and device design. The adoption of thin-film silicon-on-insulator (SOI) devices that combine high drive frequency and low drive voltage is regarded as a promising solution[1].

Today, many semiconductor wafer manufacturers and semiconductor device manufactures are engaged in the development of SOI wafers and thin-film SOI devices, respectively. In Nippon Steel Corp., work was started on the development of SIMOX (Separation by Implanted Oxygen) wafers in 1989 and efforts have been made to improve the quality and manufacturing technology of SIMOX wafers while supplying samples to users. This paper describes the characteristics of SIMOX technology and the current quality of SIMOX wafers.

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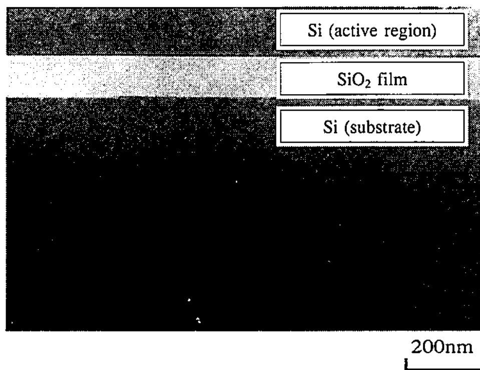


Photo 1 Cross-sectional structure of SOI wafer (SIMOX wafer)

2. SIMOX Technology

A SOI wafer is shown in **Photo 1**. The thin single-crystal silicon layer that becomes the active region where a device is to be fabricated is completely separated from the substrate silicon by an insulating film. The SIMOX wafer is one type of SOI wafer. SIMOX wafers are produced by ion implanting oxygen into a silicon wafer, heat treating the silicon wafer to induce the reaction between the silicon and oxygen and forming an insulating silicon dioxide film (buried oxide film) in the silicon wafer. As compared with other methods like bonded SOI wafers, the SIMOX wafer technology is characteristic in that it can produce silicon layers with a thickness of 200 nm or less and with extremely good thickness uniformity as required for low-power CMOS devices.

Historically speaking, a process was first developed for implanting such a dose that the oxygen to silicon concentration ratio became $C_0/C_{Si} \geq 2$[2,3]. The SIMOX thus produced is called high-dose or standard-dose SIMOX. The process was exploited to study SOI devices and to manufacture SOI devices for space and military applications. The process has the problems of 10^6 to 10^8 dislocations per square centimeter occurring in the surface Si layer and Si particles remaining in the buried oxide film. In 1990, it was found that ion implantation at such an oxygen dose as to make $C_0/C_{Si} < 2$ reduced the dislocations in the surface Si layer to 10^1 to 10^3 per square centimeter and created a region where Si particles were eliminated from the buried oxide film[4,5]. Thus was born the low-dose SIMOX technology. The oxygen dose of low-dose SIMOX was lowered to about one-fifth of that of high-dose SIMOX. The low-dose SIMOX technology eliminated obstacles to the commercial application of SIMOX wafers, or improved the quality of the top Si and the buried oxide, and reduced the manufacturing cost.

3. Low-Dose SIMOX Manufacturing Technology

3.1 Manufacturing process

Fig. 1 schematically illustrates the low-dose SIMOX manufacturing process. Oxygen ion implantation and annealing are major process steps. In the oxygen ion implant stage of the low-dose SIMOX technology*1, oxygen is distributed as supersaturated solute oxygen or minute oxygen precipitates, and is not yet transformed to a buried oxide film. Oxygen precipitates are grown by annealing and are then coalesced to form a continuous buried oxide film. In the oxygen ion implantation step, oxygen

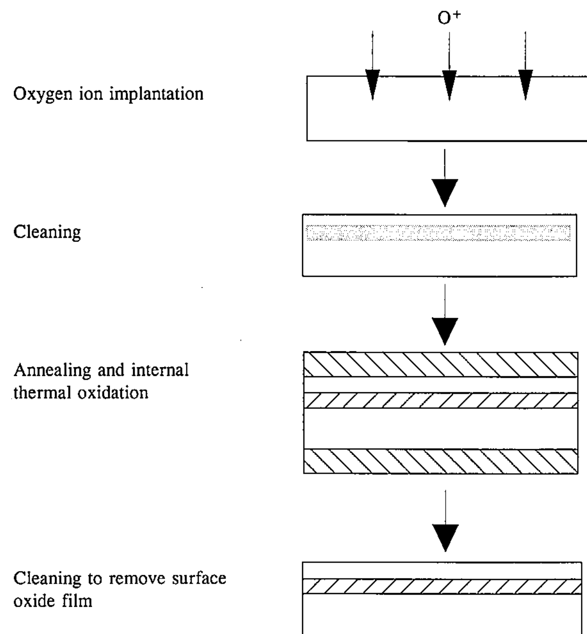


Fig. 1 Schematic illustration of low-dose SIMOX wafer manufacturing process

precipitates are not allowed to form the buried oxide. This facilitates the diffusion of point defects and inhibits the formation of dislocations. The annealing step plays a role in helping the surface silicon single-crystal layer to recover from ion implant damage.

3.2 Oxygen ion implantation technology

The oxygen ion dose and substrate temperature are important parameters that govern the distribution of initial oxygen precipitates as a source of the buried oxide and the formation of the continuous buried oxide that does not contain Si particles. The optimum dose lies between 3.0×10^{17} and 4.5×10^{17} ions/cm^2 when the implant energy is 180 keV[5,6]. **Fig. 2** shows the effect of the

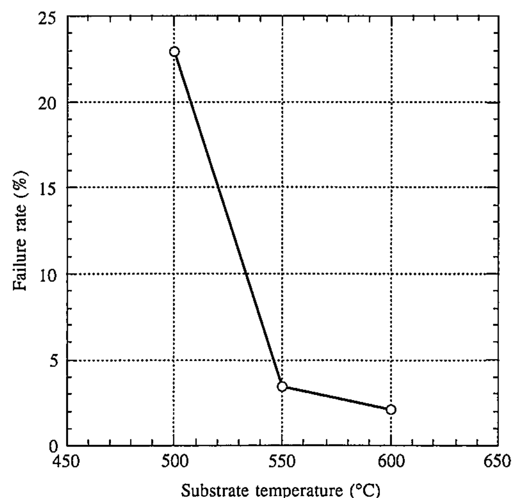


Fig.2 Effect of substrate temperature during ion implantation on leakage failure rate of buried oxide[6]

substrate temperature on the current leakage failure rate of the buried oxide. It is clear that a buried oxide with low leakage current is obtained when the substrate temperature is 550°C or more[6].

A film thickness uniformity of ±2 nm must be achieved for fully-depleted device applications. This calls for the fluctuations of the average range and the dose of oxygen ions to be controlled to ±0.5% and ±2%, respectively. To meet these exacting uniformity requirements, full attention is paid to accuracy and stability of the ion beam acceleration power supply, accuracy of dose measurement, uniformity of ion beam scanning, prevention of channeling, and uniformity of the temperature distribution in the substrate surface.

Since the dose is 1,000 times higher than used for ion implantation in conventional semiconductor processes, it is of extreme importance to reduce metal contamination and particles. As shown in **Fig. 3**, particles deposited on the wafer surface block the oxygen ions, locally produce buried oxide defects called pipes, and cause current leakage[6]. Ion implanters incorporate various measures to prevent metal contamination and particle generation, such as prevention of direct contact between the ion beam and the chamber wall.

3.3 Annealing technology

High-temperature annealing is required to ensure the full coalescence of oxygen precipitates. **Fig. 4** shows the effect of the annealing temperature on the current leakage failure rate of the buried oxide. Annealing at or above 1,330°C yields a buried oxide with little current leakage[6]. Internal oxidation is a technology for bringing the dielectric strength of the buried oxide closer to that of a thermal oxide and improving the roughness of the interface between the buried oxide and the top silicon[7]. When the SIMOX wafer is annealed in an oxygen atmosphere the oxygen dissolved from the atmosphere into the wafer causes the oxidation reaction at the interface between the top silicon and the buried oxide and forms a thermal oxide at the interface as shown in **Photo 2**. The internal thermal oxide may have a few oxygen lattice vacanices[8], but features dielectric strength close to that of the oxide at the silicon surface[9]. Internal thermal oxidation also oxidizes and reduces minute pipes and Si particles as shown in **Fig. 5**[9]. In this way, the internal thermal oxidation technology is important for the low-dose SIMOX technology.

Since the mechanical strength of silicon crystals drops at high temperatures of 1,300°C and above, special care is exercised with respect to temperature homogenization and wafer support, and the formation of slip dislocations is thus prevented.

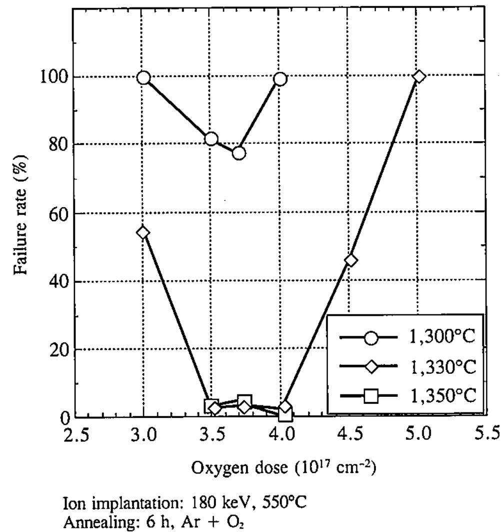


Fig. 4 Effects of annealing temperature and oxygen dose on leakage failure rate of buried oxide[6]

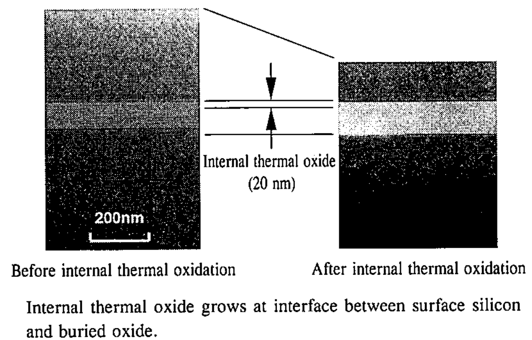


Photo 2 Growth of buried oxide by internal thermal oxidation

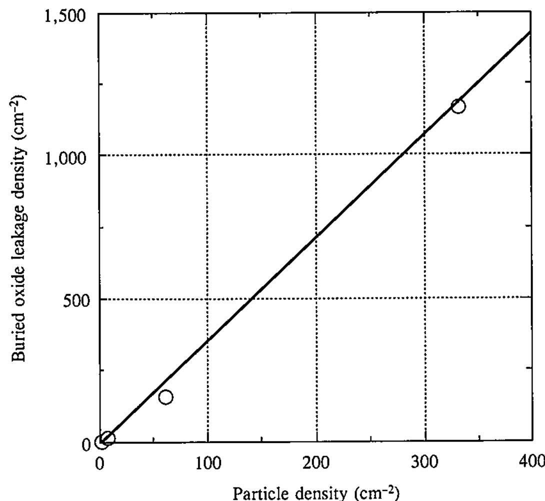


Fig. 3 Relationship between leakage density of buried oxide and density of particles deposited on wafer during oxygen ion implantation[6]

4. Quality of Present SIMOX Wafers

4.1 Film thickness uniformity

Of thin-film SOI devices, the transistor threshold voltage of fully-depleted MOS devices depends on the SOI film thickness[10]. This points to the great importance of film thickness uniformity. The surface silicon film and buried oxide film thickness distributions measured in an 8-inch SIMOX wafer by spectroscopic ellipsometry are shown in **Figs. 6** and **7**, respectively. The film thickness uniformity (maximum thickness minus minimum thickness) is 3 nm for the top silicon and 2 nm for the buried oxide. These film thicknesses uniformities are the best for SOI wafers and fully meet the film thickness uniformity requirements of devices. The

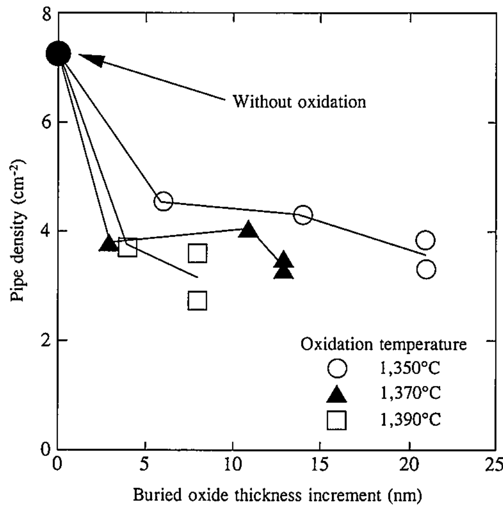


Fig. 5 Dependence of pipe density of buried oxide on increment in buried oxide thickness with internal thermal oxidation[9)]

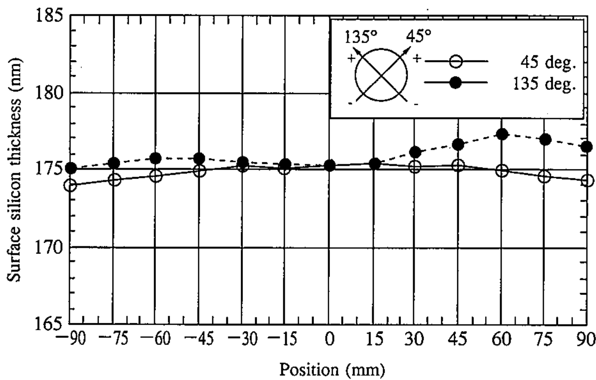


Fig. 6. Surface silicon thickness distributions in 8-inch low-dose SIMOX wafer

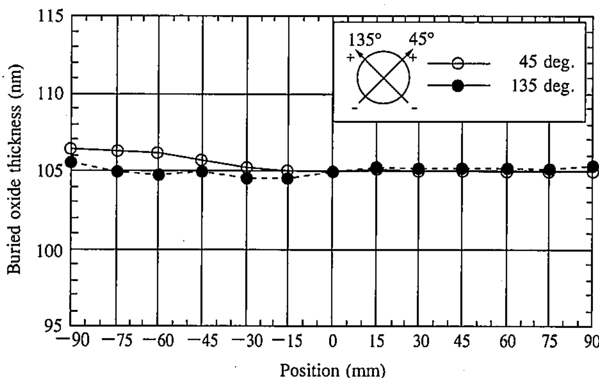


Fig. 7. Buried oxide thickness distributions in 8-inch low-dose SIMOX wafer

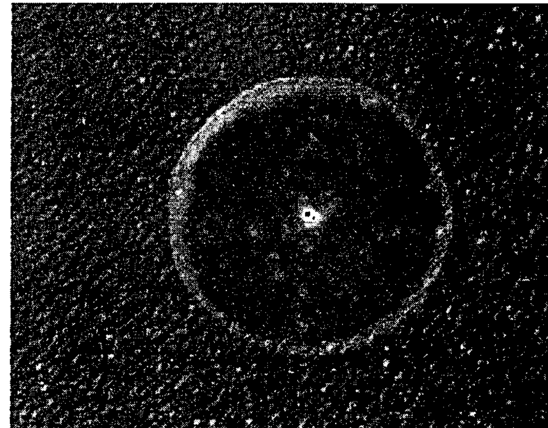
variations of average film thickness between lots are within 4 nm for both surface silicon layer and buried oxide film.

4.2 Crystallinity

The main types of crystal defects observed in the surface silicon layer of a SIMOX substrate are threading dislocations and HF defects. The density of threading dislocations revealed by Secco etching is $1 \times 10^3/cm^2$ or less. At present threading dislocations have no clear effects on device characteristics. When a SIMOX substrate is immersed in hydrofluoric acid (HF), the lower buried oxide film is etched through defects in the top silicon layer, as shown in **Photo 3**. Such defects causing the buried oxide etching are called HF defects. Metal silicides are blamed for the HF defects[11)]. With similar defects observed in bonded SOI substrates, the HF defects may be crystal defects like voids and oxygen precipitates. The HF defects are known to degrade gate oxide integrity and must be reduced to $1/cm^2$ or less. The present HF defect density ranges from 0 to 1 per square centimeter.

4.3 Contamination

Table 1 illustrates the analytical results of metal impurities in low-dose SIMOX substrates. The TXRF values are those obtained by the total-reflection X-ray fluorescence analysis of the surface of the top silicon layer in a SIMOX wafer. The VPD ($HF \cdot HNO_3$)-AAS values are determined by decomposing the surface silicon of the SIMOX wafer with $HF \cdot HNO_3$ vapor, recovering the conden-



50μm

Buried oxide is etched in circular form with HF defects as center

Photo 3 HF defects in surface silicon layer

Table 1 Metal impurities in low-dose SIMOX wafers

(Unit: 10^{10} atoms/cm^2)

Analytical method	Al	Na	Cr	Cu	Fe	Ni
TXRF	–	–	<0.25	<0.18	<0.27	<0.28
VPD($HF \cdot HNO_3$)-AAS	ND (<3.2)	0.7*	ND (<0.17)	ND (<0.42)	ND (<0.13)	ND (<0.91)

*Probably due to contamination during analysis
VPD : Vapor Phase Decomposition, AAS : Atomic Absorption Spectrophotometry
TXRF : Total reflection X-Ray Fluorescence spectrometry
ND : not determined

sate, and analyzing the condensate with an atomic absorption spectrophotometer. The prevention of metal contamination in the oxygen ion implanter and the high-temperature annealing furnace brings the cleanliness of SIMOX substrates closer to that of bulk substrates.

4.4 Dielectric strength of buried oxide

The defects (pipes) in the buried oxide degrade the function of the SOI wafer and cause the failure of MOS devices. The pipe density can be simply measured by the copper plating method as shown in **Photo 4**, and presently ranges from 0.5 to 2 per square centimeter. The pipe density must be reduced to 0.1 or less per square centimeter for LSI applications. This reduction in the pipe density is the largest problem of low-dose SIMOX wafers. **Fig. 8** is a histogram of dielectric breakdown voltage of a 102 nm buried oxide as evaluated using MOS capacitors with an area of 0.785 mm^2 each. The average breakdown voltage is about 55 V and is high enough for LSIs driven at 3 V or lower voltage. The dielectric breakdown voltage is increased by about 10 V each time the internal thermal oxide is added by 10 nm.

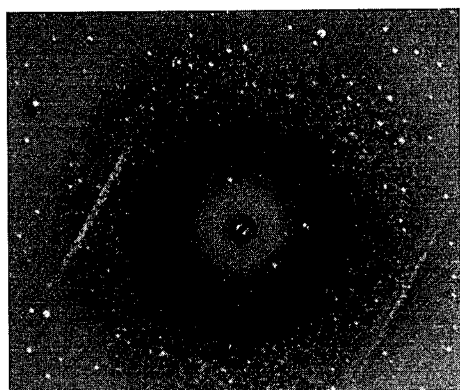


Photo 4 Copper precipitates on pipes in buried oxide as revealed by copper plating method

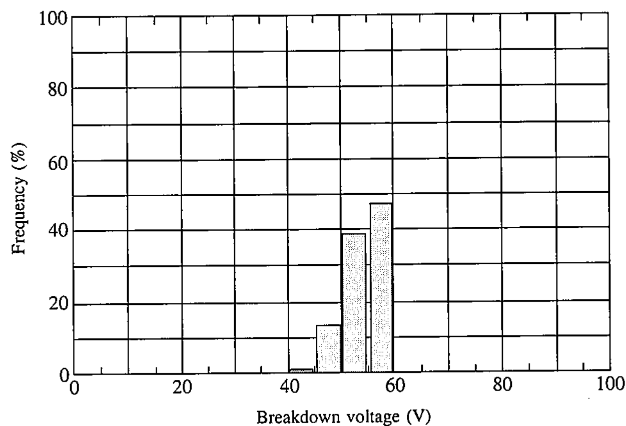
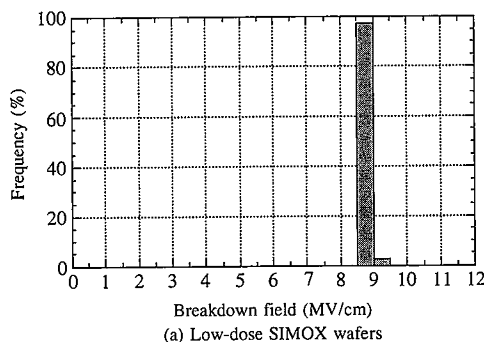


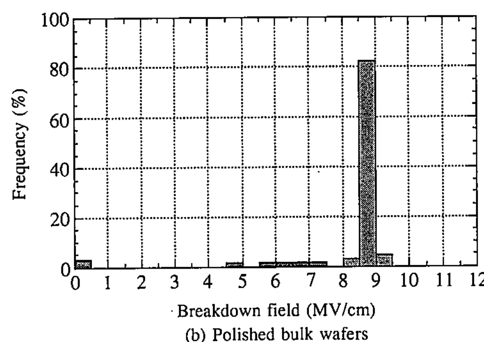
Fig. 8 Histogram of dielectric breakdown voltage of buried oxide in low-dose SIMOX wafers

4.5 Gate oxide integrity

Gate oxide integrity, the most important quality parameter of MOS devices, was evaluated by TZDB (time-zero dielectric breakdown) and TDDB (time-depended dielectric breakdown)[12]. The TZDB test method applies a ramped voltage to a gate oxide and evaluates the dielectric strength of the gate oxide. The TDDB test method evaluates the deterioration in the dielectric strength of a gate oxide under voltage or current stress by the total charge Q_{bd} applied to the gate oxide until its breakdown. To eliminate irradiation damage in the process, impurity doping was performed by diffusion, and wet etching was employed.

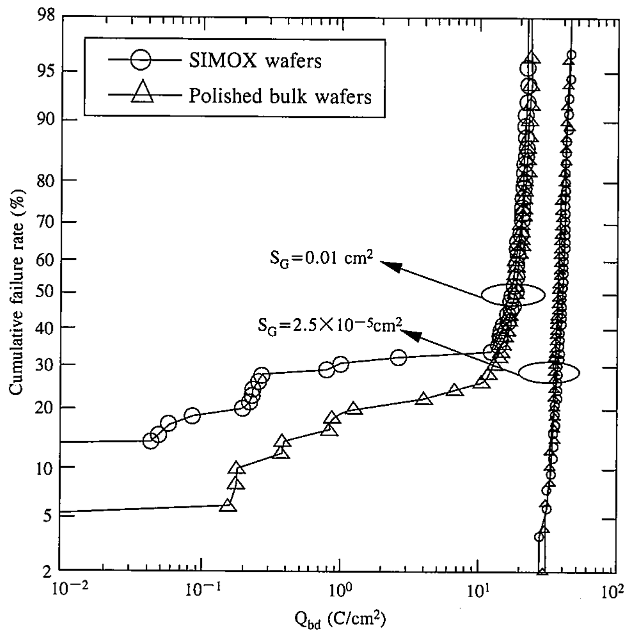
The dielectric breakdown field histograms of 24 nm gate oxides in SIMOX wafers and polished bulk wafers are compared in **Fig. 9**[13]. The dielectric breakdown current is 1×10^{-4} A/cm^2. The SIMOX wafers are free from breakdowns at 4 to 8 MV/cm, which are called mode B breakdowns and observed in the bulk wafers. Grown-in defects in the silicon crystal are said to be responsible for the mode B failures[14]. High-temperature annealing to which the SIMOX wafers are subjected in the fabrication process is considered to have reduced and eliminated the grown-in defects that otherwise lower the dielectric strength of the gate oxide in the SIMOX wafer. **Fig. 10** shows the TDDB characteristics of 8.5 nm gate oxides in the SIMOX wafers and the polished bulk wafers[13]. Although the random failure rate of SIMOX wafers is slightly higher than that of bulk wafers when the gate area is large, the SIMOX wafers have TDDB characteristics practically equal to those of the bulk wafers. Nippon Steel's SIMOX wafers are not inferior to bulk wafers in gate oxide integrity, which is a property peculiar to materials that do not deteriorate in the process concerned.





Gate oxide thickness: 24 nm
Breakdown current: 1×10^{-4} A/cm^2

Fig. 9 Dielectric breakdown field of gate oxide



Comparison of low-dose SIMOX wafers and bulk wafers
Gate oxide thickness: 8.5 nm, Constant-current stress: 5 mA/cm²

Fig. 10 TDDB characteristics of gate oxide[13)]

5. Future Problems

5.1 Reduction in pipe density of buried oxide

The most important problem is the reduction in the pipe density of the buried oxide as noted above. The pipe density must be reduced to 0.1/cm² or less for low-power LSIs to achieve a chip yield of 90 per cent or more and must be reduced to 0.01/cm² or less for 1-Gbit DRAMs. It is made clear that pipes caused by 0.3 μm and smaller particles can be removed by internal thermal oxidation to increase the buried oxide thickness to about 20 nm[9)]. We will improve the oxygen ion implanter to remove all sources of particles larger than 0.3 μm and to realize a pipe density of 0.1/cm² or less by the end of 1997.

5.2 Reduction in production cost

Now that the solution of quality problems has come into view, cost reduction has arisen as an important issue. The manufacturing cost of SIMOX wafers must be cut down to offer them at prices acceptable to customers. **Table 2** lists the factors helpful in reducing the manufacturing cost of SIMOX wafers. Scale-up is most important, followed by automation and parallel operation of multiple production units. The increase in throughput depends to a great extent on the development efforts of equipment manufacturers, including the increase in the current of oxygen ion implanters. The effectiveness of parallel operation of multiple production units depends on the production of SIMOX wafers or the demand for SIMOX wafers. This mode of operation will become markedly effective when SIMOX wafers are manufactured at a rate of 100,000 per year.

6. Conclusions

Table 3 summarizes the current quality properties of low-dose SIMOX wafers. The low-dose SIMOX wafers meet the quality requirements of thin-film SOI devices, except for the problem of buried oxide pipes. This is verified by the fact that communication LSIs test-fabricated with 120,000 gates on 0.25-μm rules by using low-dose SIMOX wafers demonstrated high speed and low power consumption as originally expected[15)].

The development of thin-film SOI devices has made remarkable progress in recent years. That the stable supply of SIMOX wafers with excellent quality is thought to be one contributing factor. Further efforts will be made to meet the ever increasing quality and cost requirements of customers.

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Table 2 Factors contributing to cost reduction of SIMOX wafers

Factor
1. Increase in yield
2. Decrease in equipment cost
3. Increase in equipment processing capability (throughput)
4. Automation and parallel operation of multiple production units
5. Increase in equipment availability and decrease in maintenance time

Table 3 Quality of low-dose SIMOX wafers

Item		Value	Method
Surface Si thickness uniformity (maximum − minimum)	(nm)	<4	Spectroscopic ellipsometry
Buried oxide thickness uniformity (maximum − minimum)	(nm)	<4	Spectroscopic ellipsometry
Crystal defects (Secco EPD)	(cm⁻²)	<1,000	
Crystal defects (HF EPD)	(cm⁻²)	0-1	
Buried oxide pipes	(cm⁻²)	0.5-2	Copper plating
Metal contamination on Si surface	(atoms/cm²)	<1×10¹⁰	Total-reflection X-ray fluorescence spectroscopy
Metal contamination in surface Si film	(atoms/cm²)	<5×10¹⁰	Atomic absorption spectrophotometry
Microroughness at Si surface, Ra	(nm)	0.4	Atomic force microscopy
Microroughness at Si/BOX interface, Ra	(nm)	0.5	Atomic force microscopy
Slip dislocations	(cm)	<3	X-ray Lang camera
Warp	(μm)	<30	8-inch wafer
Dielectric strength of buried oxide, V_{bd}	(V)	>45	BOX capacitor
Fixed charge in buried oxide, Q_{fx}	(cm⁻²)	<5×10¹⁰	BOX capacitor
Dielectric strength of gate oxide, E_{bd}	(MV/cm)	>8	MOS capacitor
Time-dependent dielectric strength of gate oxide, Q_{bd}	(C/cm²)	>20	MOS capacitor

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*1 Nippon Steel has the SIMOX substrate manufacturing technology transferred from NTT.