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Silicon Crystals with Excellent Gate Oxide Integrity

Masami Hasebe*1
Katsuhiko Nakai*1
Masamichi Okubo*2
Toshio Iwasaki*2
Yasuo Tsumori*2

Abstract:

Two types of defects degrade the dielectric strength of gate oxide films (gate oxide integrity) in silicon single crystals grown by the Czochralski pulling process. One type is grown-in defects detected as crystal-originated pits (COPs) and optical precipitate profiler (OPP) defects. The other type includes oxygen precipitates that are relatively large size and stable at high temperatures, and secondary defects arising from the oxygen precipitates. Silicon single crystals with excellent gate oxide integrity (GOI) have been successfully developed by controlling the crystal cooling conditions during the growth and reducing the number of defects that deteriorate the GOI of the crystal.

1. Introduction

Semiconductor devices have greatly advanced in circuit density, but they still follow the conventional generation change rule of about every three years. Today, 64-Mbit semiconductor memories (dynamic random access memories or DRAMs) are being mass produced. Improving the quality of silicon single crystals as substrate wafers is being demanded, along with increasing the circuit density of devices. The dielectric breakdown of transistor gate oxide films became a problem a few years ago when the mass production of 4-Mbit DRAMs was taken over by that of 16-Mbit DRAMs. The gate oxide film thickness dropped below 20 nm. The minute defects, present in silicon crystals and ignored in the past, started to exert an adverse effect on the silicon single crystals. This report describes the technology developed to control the distribution of grown-in defects in silicon crystals grown by the Czochralski process, thereby reducing the dielectric breakdown of the gate oxide film that has become a problem in the increasing circuit density of devices.

Silicon single crystals are often compared to ideal perfect crystals without dislocations. When single-crystal silicon is grown from a melt, however, point defects (vacancies, interstitial atoms, and impurity atoms) are introduced. These point defects aggregate and separate and form minute crystal defects as the crystal is cooled in the growth process. The latter defects are referred to as grown-in defects. Czochralski-grown silicon crystals, used as substrates for most of today's semiconductor devices, are produced using high-purity quartz crucibles. Upon cooling silicon single crystals contain nearly 10^{18} cm^{-3} (about 20 ppm) of oxygen atoms in an almost uniformly supersaturated condition. This impurity oxygen readily precipitates in the crystal during heat treatment. The control of oxygen precipitates in the heat treatment step of the device fabrication process has traditionally been an important issue.

Impurity oxygen in silicon wafers has the advantages of increasing the strength of the silicon wafer[1] and trapping trace metal impurities in strain fields around precipitates. This effect is commonly called the gettering effect[2]. When oxygen precipitates are present in unnecessarily large amounts, secondary defects like dislocation loops are produced and the strength of the silicon wafer is reduced. There is the additional disadvantage of degrading the junction leakage and other electrical properties of transistors[3]. It is necessary to control the oxygen concentration and precipitation to suit the device fabrication process in question.

*1 Technical Development Bureau
*2 NSC Electron Corporation

The distribution of oxygen precipitates in the silicon wafer is not uniform under the influence of the distribution of grown-in defects, although the oxygen concentration is uniform in the wafer surface. For example, **Photo 1** shows the X-ray topograph of a wafer after heat treatment to promote precipitation (heat treatment comprising annealing in nitrogen first at 400°C for 4 h and then at 1,000°C for 16 h and hereinafter called precipitation annealing). A black region, where the oxygen precipitate density is low, is distributed as a ring at about a half of the wafer radius[4,5]. The ring region marks the boundary across which the oxygen precipitate density varies greatly. This finding shows that grown-in defects to serve as oxygen precipitation nuclei are produced in a large number inside of the ring and in a smaller number outside of the ring. Control of the defect distribution immediately after growth is as important as control of the oxygen concentration in controlling the precipitation of oxygen.

The ring-like defect distribution changes with crystal growth conditions, moves toward the crystal surface with increasing growth rate, and eventually disappears into the crystal ingot surface[5]. The wafer shown in **Photo 1** was grown at a slower rate than ordinary wafers. At the rate of about 1 mm/min or more at which silicon single crystals are generally produced, the ring-like defect region is lost into the crystal periphery surface, and the ring-like defect distribution is absent in commercial Czochralski-grown silicon wafers.

In the recent increase of device circuit density, the temperature of the device fabrication process has been lowered in order to enhance the controllability of decreasing layer thickness and size and to prevent the unnecessary occurrence of crystal defects. Therefore, oxygen precipitation has been decreasing in size and amount. The distribution of defects after crystal growth is thus considered to be delicately reflected in the device fabrication yield. As described in the following chapter, the poor gate oxide integrity (GOI) of crystal wafers correlates to the formation of grown-in defects in as-grown crystals where oxygen precipitation is not progressed much. Its control has become an important issue.

2. Gate Oxide Integrity and Grown-in Defects

The crystal dependency of gate oxide dielectric breakdown was reported first by Yamabe and Taniguchi[6]. The evaluation device we used had a 25-nm thick thermal oxidation film formed on a p-type silicon wafer, 20-mm² electrodes (of high-concentration dopant polysilicon) formed on the thermal oxidation film, and ohmic contact gold deposited at the back surface of the wafer (metal oxide semiconductor capacitors). Voltage was applied between the electrodes and back-surface ohmic contacts in such a changing manner that the electric field of the gate oxide film increased at steps of 0.25 MV/cm per 200 ms. The resultant current-voltage characteristics were investigated. The voltage at which the current density of the oxide film reached a threshold of 1 μA/cm² was taken as the breakdown voltage. The electric field applied to the oxide film was obtained from the breakdown voltage. The magnitude of the breakdown electric field is known to vary with the cause of dielectric breakdown.

The mode of dielectric breakdown is classified into three types according to the dielectric breakdown electric field strength. The first is called mode A. In such an electric failure mode the dielectric breakdown occurs at a low electric field strength of 4 MV/cm or less. Foreign particles and contaminants on the wafer are blamed for mode A. The second is called mode B. Dielectric breakdown occurs at an electric field strength of 4 to 8 MV/cm. Mode B is considered as the cause for the poor long-term reliability of devices. This mode B failure is caused by crystal defects in silicon wafers. The last is the mode C region where the dielectric breakdown occurs at an electric field strength of 8 MV/cm or more. This is classified as intrinsic dielectric breakdown region. One guideline for improving the dielectric strength of the oxide film is to reduce the mode A failure (initial failure) and mode B failure.

The laser particle counter originally designed to measure foreign particles on the wafer surface has improved in accuracy. One can now detect such foreign particles as crystal-originated pits (COPs) left on the wafer surface after the wafer is given preshipment cleaning in a 1:1:5 mixture of ammonia water, hydrogen peroxide water, and pure water at a temperature of 80 to 90°C for about 20 min this cleaning is referred to as SC1 cleaning[7]. **Photo 2** shows an atomic force microscope (AFM) image of pits detected as COPs. The method of projecting an infrared laser beam into a silicon crystal and detecting scattered light from defects in the silicon crystal also has improved in sensitivity to locate minute grown-in defects.

The density and size of grown-in defects was quantitatively analyzed by using infrared-laser bright-field interferometry. A commercial instrument based on this principle is known as an opti-

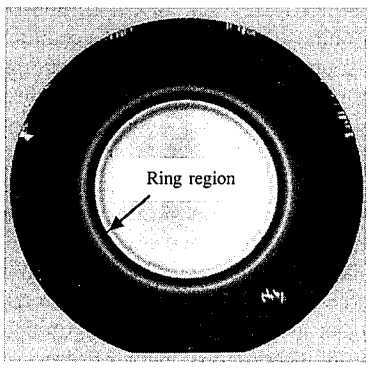


Photo 1 X-ray topograph of 6-inch Czochralski-grown silicon wafer with ring region after heat treatment in nitrogen at 800°C for 4 h and at 1000°C for 16 h

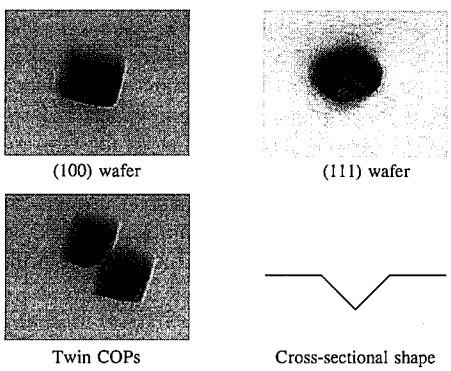


Photo 2 AFM images of COPs on mirror wafer after cleaning (by courtesy of Seiko Instruments Inc.)

cal precipitate profiler or OPP[8]. Crystal wafers grown under different conditions were used as samples. The samples were subjected to the iteration of the SC1 cleaning and COP measuring, and evaluated as to the number density of grown-in defects. The dielectric breakdown of MOS (Metal Oxide Semiconductor) capacitors was investigated by changing the area of evaluation electrodes. The correlation between the number density of COPs and the number density of defects obtained from dielectric strength measurement is shown in **Fig. 1**. The correlation between the number density of defects measured with the OPP and the average mode B failure rate is shown in **Fig. 2**. The number density of COPs is related to the number density of dielectric breakdown defects in an almost 1:1 proportion. This means that the COP defects is correlated very well with poor gate oxide integrity. The number density of OPP defects is practically the same as that of COP defects. This means that the mode B failure rate increases with increasing OPP defect density.

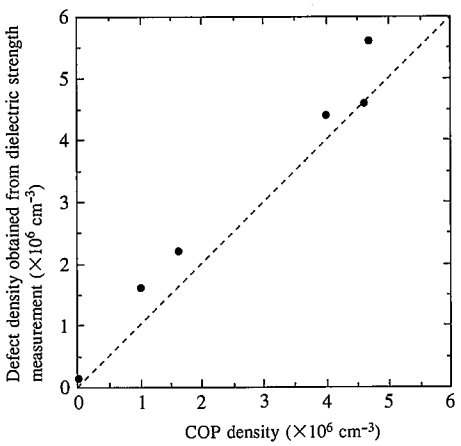


Fig. 1 Correlation between number density of COP defects after repeated SC1 cleaning and density of dielectric breakdown defects obtained from dielectric strength measurement

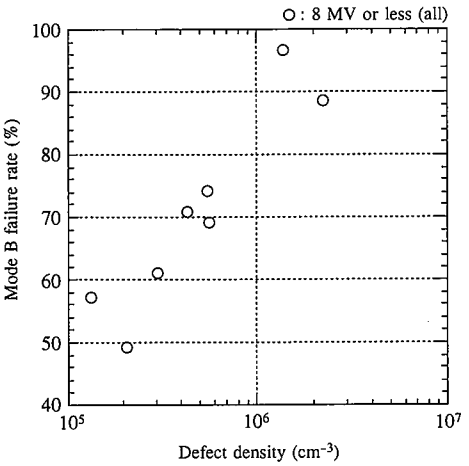


Fig. 2 Correlation between COP defect density and dielectric breakdown of 8 MV/cm or less

3. Effects of Cooling Conditions of Growing Crystals on Grown-in Defects and Gate Oxide Integrity

The cooling conditions of crystals during their growth was observed, and the effects of varying cooling conditions on the formation of grown-in defects and the oxide gate integrity of the grown crystals was investigated. To clarify the effect of temperature on crystals during their growth, the growth rate of the crystals was extremely reduced midway during their growth. The crystals which were held at the temperatures where their portions would be exposed in the pulling furnace (hereinafter the crystals are called the furnace-held crystals), were investigated for the distribution of grown-in defects, and evaluated as to gate oxide integrity[9,10].

To investigate oxygen precipitation behavior, rectangular samples sliced along the axis of crystal growth were given the above-mentioned precipitation annealing heat treatment. Their oxygen concentration distribution was measured by microfocus Fourier transform infrared spectroscopy (μFT-IR). To investigate the thermal stability of grown-in defects, other samples were annealed in helium at a high temperature of 1,250 to 1,350°C, were given the above-mentioned precipitation anneal to bring residual defects, and were etched by the Wright method known as a crystal defect selective etching method. The defect density of the samples obtained was then measured.

The X-ray topograph of a crystal sample held in the pulling furnace after the precipitation anneal is shown in **Fig. 3**(a). The changes in the oxygen concentration of the sample along the crystal growth axis before and after the precipitation anneal are shown in **Fig. 3**(b). **Fig. 3**(c) shows the dielectric strength of silicon crystal wafers sliced normal to the crystal growth axis and polished to mirror finish. The amount of oxygen precipitation which is the difference in oxygen concentration before and after the annealing heat treatment, is small in the region E held at 1,300°C or above. In region E the ring is eliminated at the center of the crystal. The amount of oxygen precipitation is large in the region A held at 1,300 to 1,100°C and very large in the region B held at 1,100 to 1,050°C, but smaller in the region C held at 1,050 to 1,000°C. In the region D held at 1,000°C or less, the amount of oxygen precipitation increases again. These results indicate that the temperature region of 1,100 to 1,000°C exerts a strong effect on the formation of grown-in defects to serve as oxygen precipitation nuclei.

The dielectric strength distribution does not necessarily agree with the oxygen precipitate distribution. The increase in the frequency of mode C failures and the decrease in the frequency of mode B failures (6 MV/cm or less) agree with the oxygen precipitation tendency of region B. In other words, the dielectric strength is improved in the region where the amount of oxygen precipitated by the precipitation anneal is the largest. Some portions were observed where the frequency of mode A failures increased. The frequency of mode A failures was found to increase in region C where oxygen is precipitated in small amounts.

As results of the grown-in defect evaluation, the changes in the density of COP and OPP defects in different crystal regions are shown in **Figs. 4** and **5**, respectively. **Fig. 4** shows the change in the area density of COP defects, measuring 0.11 μm or more and revealed on the wafer surface after the SC1 cleaning. **Fig. 5** shows the change in the volume density of OPP defects of detectable size, about 110 nm or more. Both COP and OPP

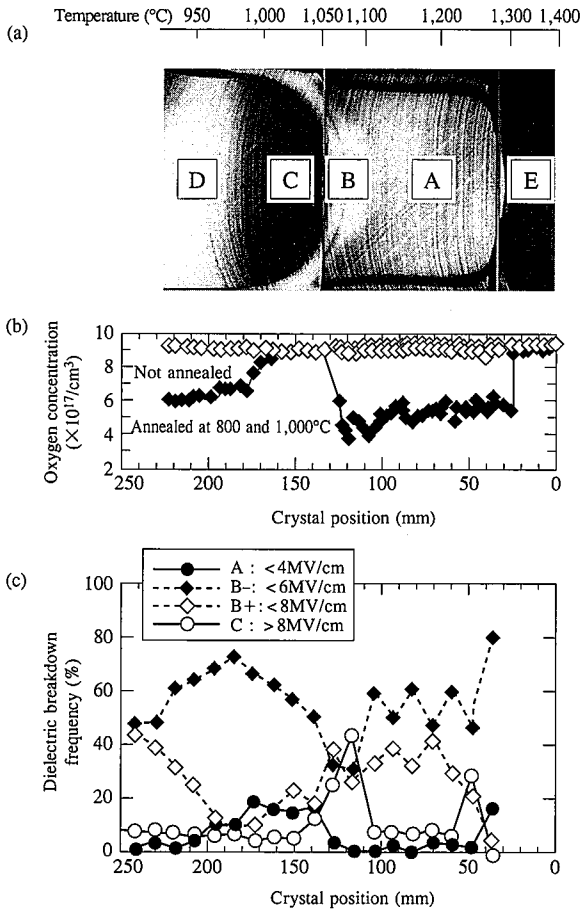


Fig. 3 X-ray topograph of furnace-held crystal after annealing at 800°C for 4 h and at 1,000°C for 16 h (a); distribution of oxygen concentration at center of crystal after annealing (b); dielectric strength measured at oxide film thickness of 25 nm (c)

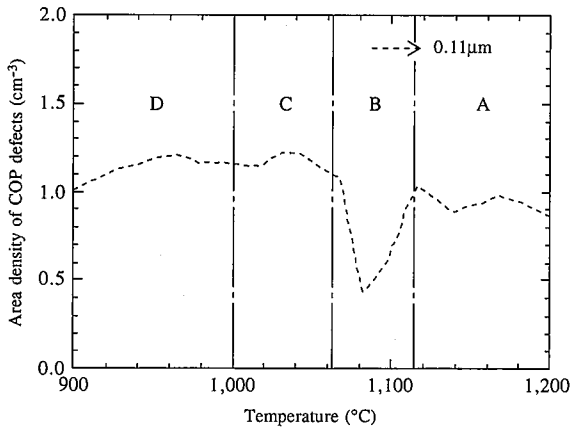


Fig. 4 Distribution of COP defects (> 0.11 μm) versus holding temperature of growth-retarded crystal

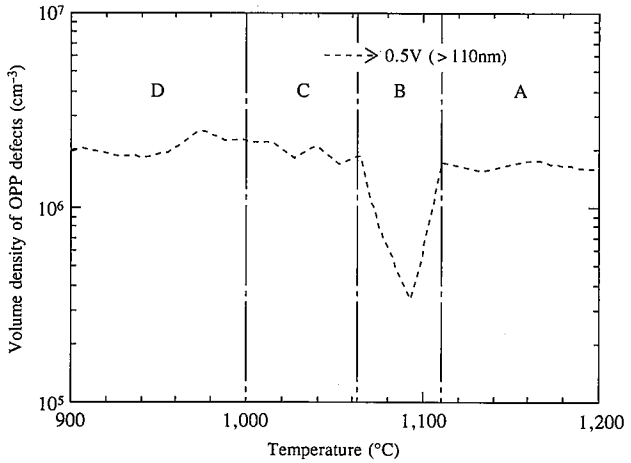


Fig. 5 Distribution of OPP defects (> 110 nm) versus holding temperature of growth-retarded crystal

defects are shown to decrease in region B where the frequency of mode C failures is increased and the dielectric strength of gate oxide is improved. This finding means that these grown-in defects are responsible for the deterioration of dielectric strength at a low mode B of 6 MV/cm or less. The dielectric strength of gate oxide is considered to have been improved by the reduction in the density of the COP and OPP defects. The grown-in defects detected as the COP and OPP defects related to mode B failures are considered as defects arising from the coalescence of point defects in silicon crystals.

No correlation with the density of grown-in defects is noticed for region C where the increase in the frequency of mode A failures and the remarkable dielectric strength degradation of gate oxide film are observed. An experimental study was conducted to clarify the difference in the state of grown-in defects between different crystal regions by annealing crystal regions at high temperatures and examining them for residual defects[11].

Fig. 6 shows the crystal center defect density and the furnace holding temperature after the furnace-held crystals were annealed at high temperatures of 1,250 to 1,350°C. Only the defect density of region B was increased by annealing at 1250°C. Annealing at 1,300°C reduced the defect density of region B to about one-tenth of that of regions A and C and left the defect density of regions A and C unchanged. The 1,350°C anneal lowered the defect density of region A to approximately the same degree as that of region B, and only slightly changed the defect density of region C. These results indicate that the thermal stability of grown-in defects increases in the order of regions B, A and C and that the most stable defects were formed in the region C held at the lowest temperature. The 1,300°C anneal destabilizes and reduces the defects in the region B where the gate oxide integrity is improved. The 1,350°C anneal allows some defects to remain in the region C where the gate oxide integrity is deteriorated.

Despite the high-temperature annealing heat treatment, stable defects are thought to be responsible for mode A failures. Crystal defects related to mode B failures and stable after high-temperature annealing were investigated as follows. Small silicon crystal blocks were first initialization annealed at 1,380°C and then heat treated to simulate a crystal holding experiment in the pulling fur-

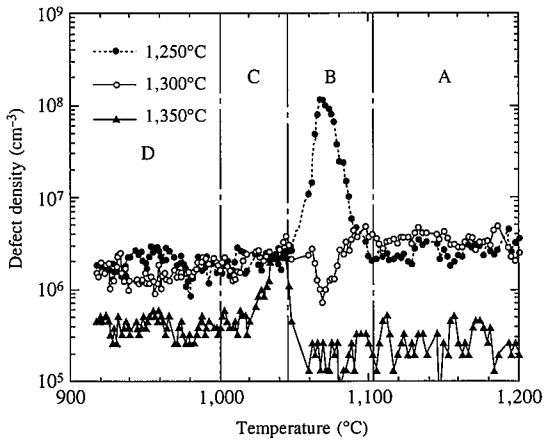


Fig. 6 Relationship between defect density and furnace holding temperature of furnace-held crystals after annealing in helium at 1,250 to 1,350°C for 2 h

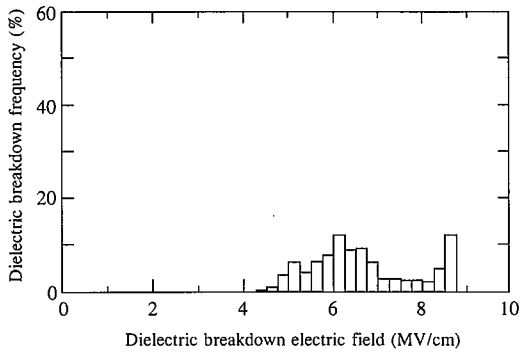
nace[9]. The samples thus obtained were observed by transmission electron microscopy. Huge plate-like oxygen precipitates 50 to 90 nm in size were observed in the simulation heat treated samples at the temperature of 1,000°C where the gate oxide integrity is markedly degraded. About one-third of the huge oxygen precipitates were found to accompany dislocation loops. The samples heat treated at 1,050°C where the gate oxide integrity is improved revealed no defects of such size range. These results suggest that the huge oxygen precipitates or dislocation loops are stable defects that do not disappear despite the high-temperature annealing heat treatment.

5. Development of Crystals with Improved Gate Oxide Integrity

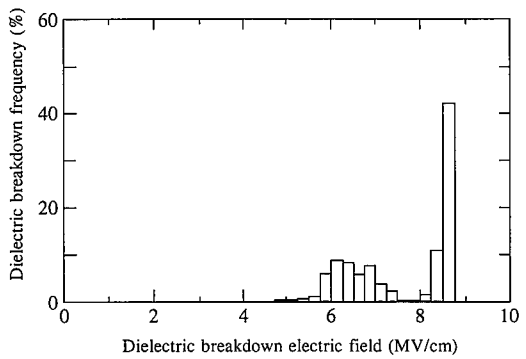
The results of the study conducted to investigate the effects of crystal cooling conditions on the grown-in defects and gate oxide integrity of silicon crystals as described show that the gate oxide integrity of silicon crystals can be improved by slowly cooling from 1,100 to 1,050°C and rapidly cooling from 1,050 to 1,000°C. Intense slow cooling in the temperature region of 1,100 to 1,050°C increases the precipitation of oxygen. Given this problem, silicon crystals must be slowly cooled to assure appropriate oxygen precipitation behavior and to improve gate oxide integrity. This temperature control led to the successful development of silicon crystals with improved gate oxide integrity as shown in **Fig. 7**. **Fig. 7**(a) shows the dielectric breakdown distribution of a wafer produced by the conventional crystal growth process, whereas, **Fig. 7**(b) shows the dielectric breakdown distribution of a newly developed wafer with improved oxide gate integrity. The newly developed wafer is found to be a good crystal without distribution of mode A and B failures at 6 MV/cm or less and with excellent gate oxide integrity.

6. Conclusions

Czochralski-grown silicon crystals with excellent gate oxide integrity have successfully been developed by controlling the cooling conditions during the growth of the silicon crystals. The key points to this success are the reduction in grown-in defects detected as COP and OPP defects and the control of the formation of



(a) Dielectric breakdown electric field and frequency histogram of conventional crystal



(b) Dielectric breakdown electric field and frequency histogram of crystal with improved gate oxide integrity

Fig. 7 Dielectric breakdown electric field and frequency histograms of conventional crystal and crystal with improved gate oxide integrity

relatively large oxygen precipitates stable at high temperatures. The increasing circuit density of semiconductor devices is expected to reveal still smaller defects as problems. Now that the mass production of 64-Mbit memories has commenced, epitaxial wafers with excellent crystal properties in the device fabrication region now have application as mass-production start-up substrates. Further improvement in quality is also required of Czochralski mirror wafers with cost advantage. These movements all call for the development of silicon crystals with the fewest possible defects.

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