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Development of GaAs-on-Si Wafers Using High-Speed Rotating-Substrate-Type MOCVD System

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Abstract:

GaAs-on-Si wafers having GaAs-AlGaAs epitaxial layers grown on a Si substrate have been developed by using a metal-organic chemical vapor deposition (MOCVD) system of the high-speed rotating substrate type. High-electron mobility transistor (HEMT) and metal-semiconductor field effect transistor (MESFET) devices have been test-fabricated to evaluate the performance of the GaAs-on-Si wafers. The results of the evaluation show that the conventional problems of the GaAs-on-Si wafers, such as high dislocation density, surface roughness, and Si auto doping, can be solved. Power MESFETs with high heat dissipation can prevent the problem of parasitic capacitance resulting from the presence of a interfacial high-electron density layer. Power MESFETs are thus considered to be close to becoming a practical application as devices for cellular phones.

1. Introduction

Optical devices, such as light emitting diodes and lasers, were main applied devices of compound semiconductors like gallium arsenide (GaAs). The popularity of cellular phones in recent years has increased the demand for GaAs field effect transistors (FETs). High-output and low-power consumption (high-efficiency) MESFETs (metal-semiconductor FETs) and HEMTs (high-electron mobility transistors) fabricated by epitaxial growth on bulk GaAs single crystal substrates (liquid encapsulated Czochralski or LEC-GaAs substrates) have been enthusiastically developed and used as FETs. The replacement of an epitaxial wafer on a LEC-GaAs substrate (GaAs-on-GaAs substrate) by a GaAs-on-Si substrate fabricated by the epitaxial growth of GaAs on a Si substrate as the substrate for these electronic devices is the purpose of the present study.

Since the GaAs-on-Si substrate innovation of 1984[1], various GaAs-on-Si applied devices have been test-fabricated and evaluated. The GaAs-on-Si wafers with excellent heat dissipation can be obtained, but have not yet been commercialized. As compared with the LEC-GaAs substrate, the GaAs-on-Si substrate has the following problems: (1) the dislocation density is high; (2) surface morphology is poor; (3) parasitic capacitance arises from the conductive GaAs interfacial layer produced by the diffusion of Si into the GaAs epitaxial layer at the GaAs-Si interface; and (4) the doping of vaporized Si from the bottom and side surfaces of the Si substrate into the GaAs grown surface takes place during the growth of GaAs.

As far as problem (1) is concerned, the high dislocation density has an adverse effect on the luminous efficiency of opto devices, and has been reduced by various methods. To achieve a dislocation density of 10^5 cm^{-2} or less, special techniques are required, resulting in lower wafer productivity and higher wafer cost. For problem (2), Fujitsu Research Laboratory pointed out that pits, one source of surface roughness, have an adverse effect on the electrical properties of HEMTs[2]. They reported that pits can be reduced by mechanically polishing a GaAs-on-Si wafer,

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regrowing GaAs on the wafer, and using the resultant epitaxial wafer with improved morphology[3]. However this procedure makes wafers prohibitively expensive for practical use. As for problem (3), the parasitic capacitance of FETs on GaAs-on-Si wafers is reported to be responsible for an increase of 10 to 20% in the delay time and decrease in the cutoff frequency as high-frequency properties as compared with FETs on GaAs wafers[4,5]. Concerning problem (4), silicon reacts with hydrogen to vaporize (form silicon tetrahydride or SiH_4) from the back surface of the GaAs-on-Si wafer. This SiH_4 contaminates the GaAs epitaxial layer, shifts the electrical conductivity of the GaAs epitaxial layer away from the design value, and deteriorates the distribution of the threshold voltage V_{th} of the FETs in the wafer. This problem has been countered by coating the back surface of the Si wafer with silicon oxide (SiO_2) by the thermal oxidation method[6]: This process also raises the cost of the wafer and induces the surface roughness of the wafer.

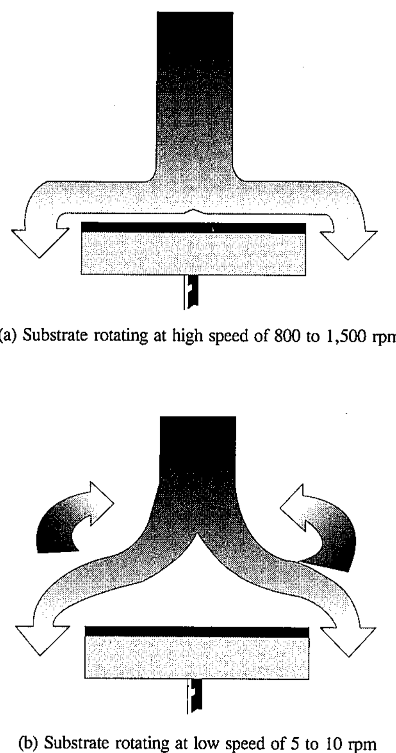
Against this background, attention was focused on the application of GaAs-on-Si wafers to surface electron devices, such as HMETs and MESFETs. They were considered less sensitive to the effect of dislocations. The metal-organic chemical vapor deposition (MOCVD) growth conditions for GaAs-on-Si wafers were optimized and the surface morphology of GaAs-on-Si wafers was improved. As described in the next chapter, it is demonstrated that the auto doping of Si can be made negligibly small without SiO_2 coating by a vertical MOCVD system of the high-speed rotating substrate type. The surface electron devices were then test-fabricated and evaluated, and it was found that the above-mentioned problems (1) and (2) do not appreciably detract from the properties of the GaAs-on-Si devices[7,8].

This paper describes the MOCVD process for the epitaxial growth of GaAs-on-Si wafers and shows that the problems with the commercialization of electron devices using GaAs-on-Si wafers can be solved as indicated by the evaluation results of test-fabricated devices. It is shown that the low cost and high heat dissipation characteristics of GaAs-on-Si wafers are advantageous for power FETs with a large gate area and that the aforementioned problem of parasitic capacitance can be solved as well.

2. Fabrication of GaAs-on-Si Wafers with Vertical MOCVD System of High-Speed Rotating Substrate Type

2.1 Characteristics of the system

Fig. 1 schematically illustrates the flow of a gas vertically blown against a substrate rotating at high speed. This is the largest characteristic of the MOCVD system[9]. The gas flow is compared in very simplified form in two cases. In one case, the substrate is rotated at a high speed of 800 to 1,500 rpm as shown in **Fig. 1**(a). In the other case, the substrate is rotated at a lower speed of 5 to 10 rpm as shown in **Fig. 1**(b). In the former case, the centrifugal force eliminates the gas flow turbulence shown in **Fig. 1**(b) and causes the gas to flow along the substrate. As a result, the gas is decomposed near the surface of the substrate by the heat of the substrate and diffused into the surface of the substrate to form a thinner diffusion layer with greater uniformity. An epitaxial layer of excellent thickness can be consequently obtained. The computational and experimental results are given in greater detail in **Fig. 2**[10]. **Fig. 3** shows the homogeneity of a GaAs epitaxial layer grown on a four-inch Si substrate. At a layer thickness of about 2.7 μm, the thickness uniformity in the GaAs epitaxial layer is a very good ±0.7% (against 1 to 3% with conventional MOCVD apparatus). As discussed in 4.1, this excellent result will be reflected in the threshold voltage uniformity of FETs.



(a) Substrate rotating at high speed of 800 to 1,500 rpm

(b) Substrate rotating at low speed of 5 to 10 rpm

Fig. 1 Gas flow around rotating substrate

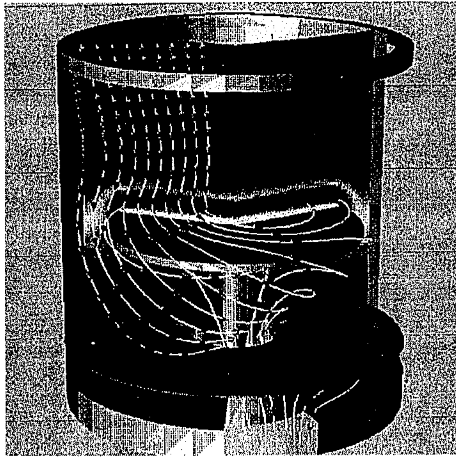
2.2 Epitaxial growth of GaAs on Si substrate

The Si (001) substrate was misoriented at 3° forward the <110> direction. GaAs and AlGaAs were epitaxially grown by the two-step growth method[1]. GaAs and AlGaAs were first grown at 400° to about 200 Å and then at 650 to 700°C to a GaAs-AlGaAs layer with a total thickness of 3.0 to 3.5 μm.

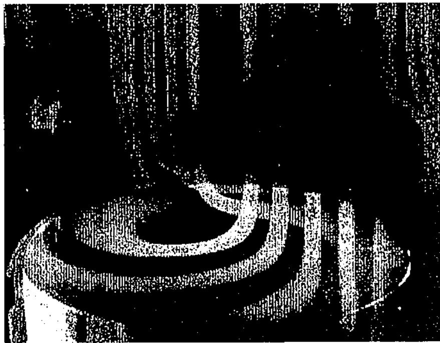
To improve surface morphorogy, growth at 600°C for a few minutes is inserted between the steps for some applications. Trimethyl gallium (TMG), trimethyl aluminum (TMA) and arsine (AsH_3) were used as raw material gases, and disilane (Si_2H_6) was used as the doping gas. When the electron concentration of undoped GaAs was evaluated by measuring C-V and other properties, the effect of auto doping from the substrate was found to be practically negligible. This is probably because the high-speed gas stream in the present system has the effect of carrying away the gases vaporized from the edges and back surface of the silicon substrate, as compared with the auto doping effect observed in horizontal growth furnaces in general use. It is thus unnecessary to coat the back surface of the wafer with SiO_2 to avoid auto doping. This is the great advantage of the MOCVD system.

2.3 Fabrication of epitaxial wafers for electron devices

The epitaxial layer structures of HEMTs, power MESFETs, and ion-implanted MESFETs on Nippon Steel's representative silicon substrates are shown in **Figs. 4**(a), **4**(b), and **4**(c), respectively. The representative carrier concentration of undoped GaAs and AlGaAs is controlled by the V/III ratio. The hole concentra-



(a) Gas flow as simulated by computer



(b) Gas flow near substrate as simulated by smoke

Fig. 2 Gas flow pattern in vertical MOCVD furnace of a high-speed rotating substrate type[10)]

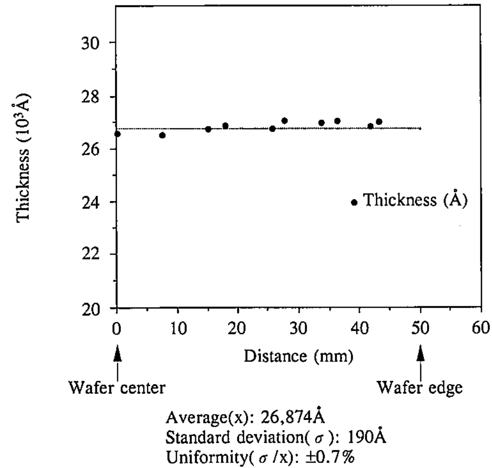


Fig. 3 Uniformity of GaAs epitaxial layer thickness on 4-inch GaAs-on-Si wafer

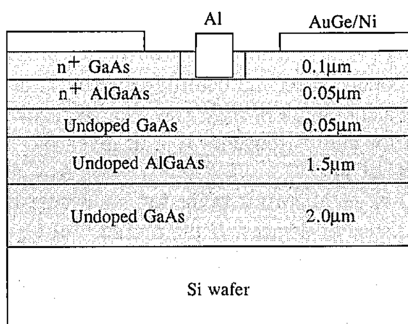
tion is $p = 8 \times 10^{14}/cm^3$ for undoped GaAs and $p = 7 \times 10^{15}/cm^3$ for undoped AlGaAs. The representative electron concentration of GaAs in the active layer of the MESFET structure is $n = 2 \times 10^{17}/cm^3$, and electron mobility at room temperature is about 3,000 cm^2/Vs. As electron mobility of GaAs channel of the HEMT structure, about 5,000 cm^2/Vs is obtained at room temperature. The AlGaAs layer effectively works in reducing the leakage current and increasing the breakdown voltage. It is indispensable for FETs on Si substrates. Without heat treatment and super lattice insertion to reduce dislocations, a dislocation density of the order of $10^8/cm^2$ penetrating to the surface is present according to etch pit and electron microscopy observations.

3. Evaluation of GaAs-on-Si Wafers with Test Fabrication of Electron Devices

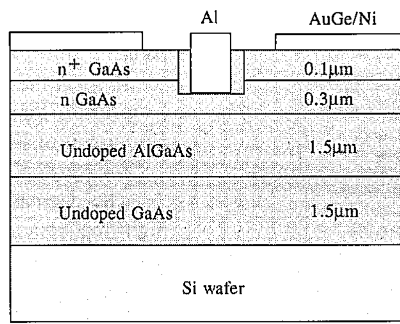
3.1 Evaluation of threshold voltage V_{th} uniformity in HEMTs and ion-implanted MESFETs

With LEC-GaAs substrates, the threshold voltage V_{th} and dislocation network of ion-implanted FETs are clearly positionally correlated to each other[11)]. Here, standard deviation of the threshold voltage σV_{th} of HEMTs (fully epitaxial process) and ion-implanted MESFETs were measured and evaluated to investigate the effects of GaAs-on-Si wafer dislocation defects and surface roughness on the properties of FETs. The epitaxial layer structures of the HEMTs and the ion-implanted MESFETs are as shown in **Figs. 4**(a) and **4**(c), respectively.

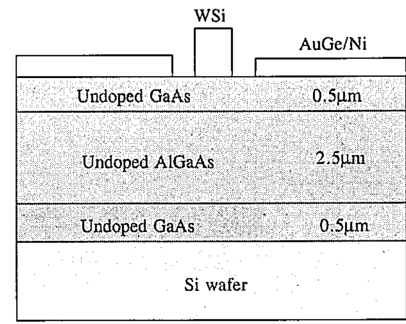
Fig. 5 shows an example of the microscopic uniformity of V_{th} in HEMTs on a Si wafer with a gate length of 1.2 μm and gate



(a)
HEMT structure



(b)
Power MESFET structure



(c)
Ion-implanted MESFET structure

Fig. 4 Epitaxial layer structures of GaAs-on-Si wafers. Electrodes after device process are shown highlighted

width of 30 μm. The σV_{th} is about 9 mV at the center of the 3-inch wafer and about 14 mV at 15 mm from the wafer edge. These values of σV_{th} favorably compare with 20 to 30 mV for GaAs ICs now on the market. No faulty devices are found within the measured range[8].

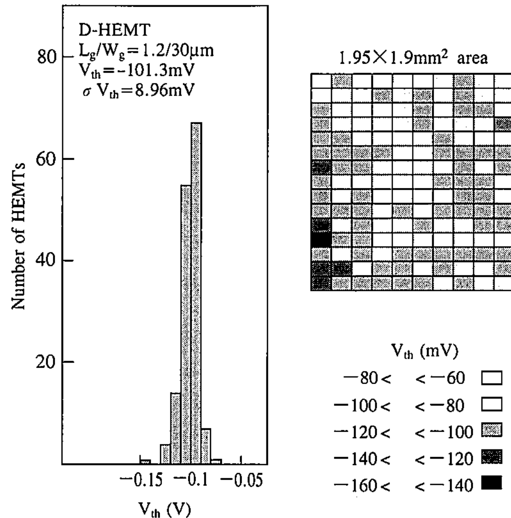


Fig. 5 Microscopic uniformity of V_{th} in HEMTs at center of Si wafer

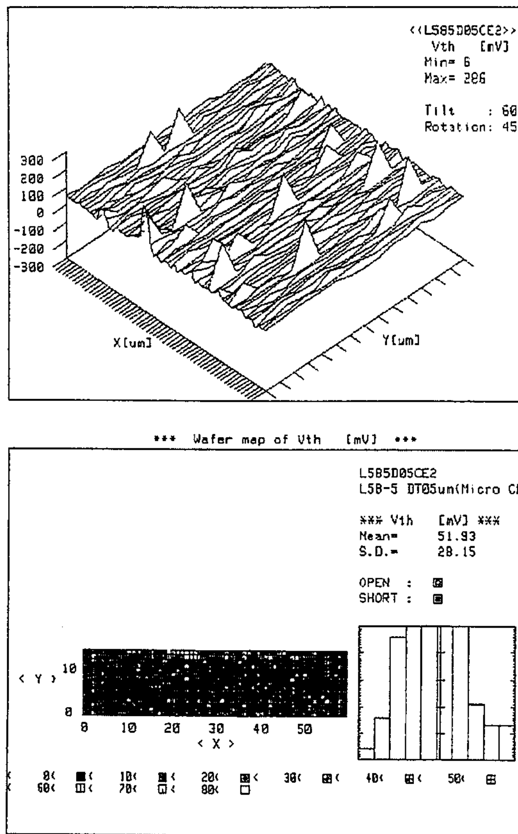


Fig. 6 Microscopic uniformity of V_{th} in ion-implanted MESFETs[13]

An example of the microscopic uniformity of V_{th} in ion-implanted MESFETs is shown in **Fig. 6**. The FET array is composed of FET elements with a gate length of 0.5 μm and gate width of 10 μm. The active layer is formed at an acceleration voltage of 30 kV and Si ion dose of $8 \times 10^{12}/cm^2$ and provided with a p-type buried layer. As can be seen from **Fig. 6**, abnormal values of V_{th}, apparently arising from the interaction with dislocations, are recognized in some portions, when the ion implantation process is used. Faulty devices (open or shorted) are also present. Consequently, σV_{th} assumes a value of 30 to 50 mV. In the past attempts were made to fabricate ICs from GaAs-on-Si wafers on a trial basis by using the ion implantation process[12]. Such ICs are not yet commercially produced, probably because the presence of faulty devices reduced yield and reliability. In recent years, however, the nonuniformity of V_{th} has been improved to a considerable degree by the method of locally applying stress near FET gates[13]. For HEMTs and digital MESFETs, entirely composed of epitaxial layers as noted above, GaAs-on-Si wafers are free from the effect of dislocations on the threshold voltage V_{th} and are not inferior to GaAs-on-GaAs wafers in yield and reliability.

3.2 Evaluation of high-frequency characteristics

The scattering (S) parameter of the above-mentioned HEMTs on silicon wafers was measured in the frequency region of 1 to 20 GHz by using a high-frequency probe. The cutoff frequency f_T at which the current gain h_{21} becomes unity and the scattering parameter of equivalent circuits built for HEMTs on Si wafers[14] were obtained from the measured results. The cutoff frequency f_T of HEMTs on Si wafers is 10 to 20% lower than that of HEMTs on GaAs wafers. This is known to result from the parasitic capacitance between the high-electron concentration layer at the interface and the metal electrodes (mainly bonding pads) at the surface. From the results of simulation, one can predict that parasitic capacitance occurs if carriers are present in $4 \times 10^{16}/cm^3$ or more at the interface[15]. When the Si substrate was removed by etching and the GaAs surface at the interface was examined by Raman spectroscopy, an electron concentration of at least $2 \times 10^{18}/cm^3$ was confirmed to be present due to the diffusion of Si into GaAs under our normal growth conditions[16].

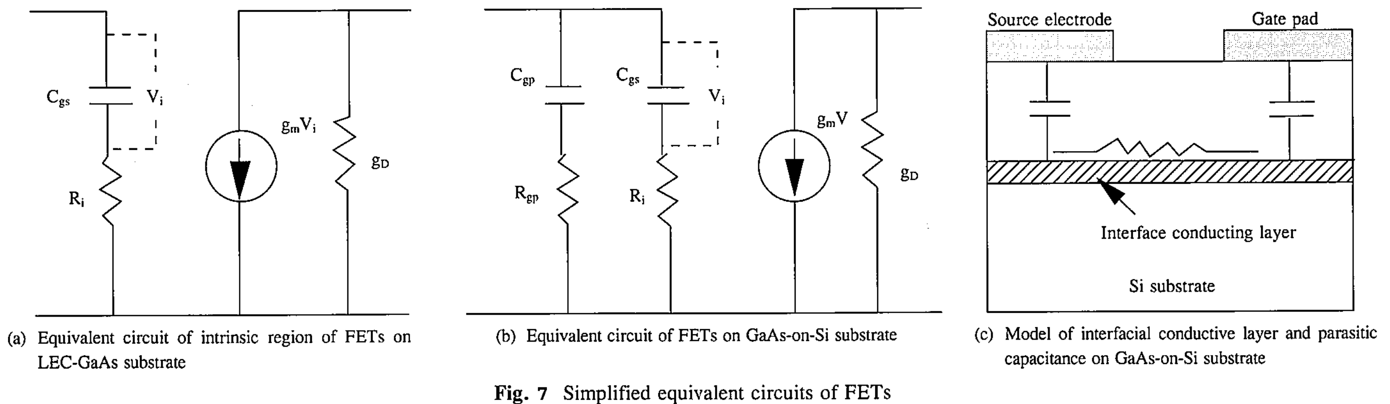
The equivalent circuit that simplifies the intrinsic region of FETs on a semi-insulating LEC-GaAs substrate is shown in **Fig. 7**(a). C_{gs}, R_i, and g_D are the gate-source capacitance, input resistance, and drain conductance, respectively. The equivalent circuit of **Fig. 7**(b) is thought to apply to FETs on a GaAs-on-Si substrate when the model of **Fig. 7**(c) is taken into account. C_{gp} and R_{gp} are the parasitic capacitance and resistance produced between the interfacial conductive layer and electrodes, especially gate pads.

If g_m is the mutual conductance, the cutoff frequency f_T is $f_T \sim g_m/2\pi C_{gs}$ for the equivalent circuit of **Fig. 7**(a). For the equivalent circuit of **Fig. 7**(b), the cutoff frequency f_T is as given by

$$f_T \sim g_m/2\pi C_{gs}(1 + C_{gp}/C_{gs}) \quad \cdots\cdots(1)$$

The decrease of C_{gp} is an important point for improving the high-frequency characteristics of devices. If the presence of C_{gp} is unavoidable for GaAs-on-Si wafers, the high-frequency characteristics of FETs on GaAs-on-Si wafers can be improved to those of FETs on GaAs wafers by increasing R_{gp} or adopting a device structure to reduce the C_{gp}/C_{gs} ratio as indicated by Eq. (1).

Most of the parasitic capacitance C_{gp} is accounted for by the contribution of the capacitance between the pads and interfacial layers. C_{gp} can be reduced by (1) making the pad area as small as



(a) Equivalent circuit of intrinsic region of FETs on LEC-GaAs substrate

(b) Equivalent circuit of FETs on GaAs-on-Si substrate

(c) Model of interfacial conductive layer and parasitic capacitance on GaAs-on-Si substrate

Fig. 7 Simplified equivalent circuits of FETs

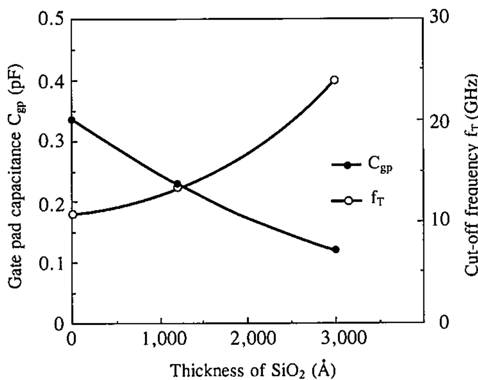


Fig. 8 Effect of thickness of SiO_2 layer inserted beneath gate pads on gate pad capacitance C_{gp} and cutoff frequency f_T

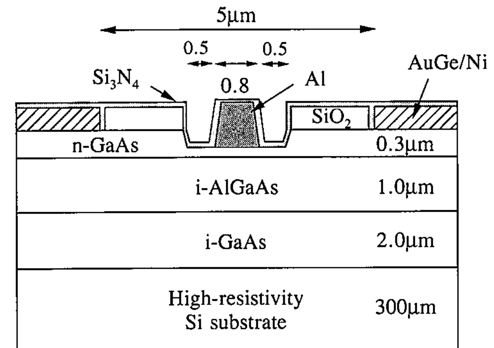


Fig. 9 Cross-sectional structure of test-fabricated power MESFETs on Si wafer

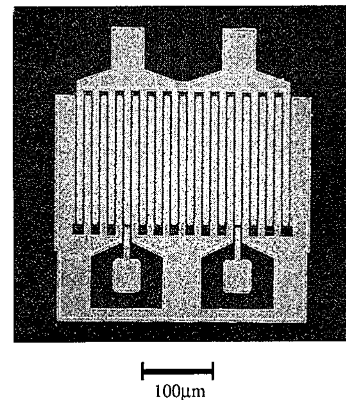


Photo 1 SEM photograph of test-fabricated power MESFETs on Si wafer

possible or (2) placing an insulating layer like SiO_2 beneath the pad metal and increasing the pad electrode-to-interfacial layer distance. C_{gp} was actually reduced by about a half by reducing the pad area from 80 to 50 μm^2 and by about another half by inserting a 0.3-µm thick SiO_2 layer. **Fig. 8** shows the experimental values of the gate pad capacitance C_{gp} and the cutoff frequency f_T when a SiO_2 layer was inserted below the gate pads. From **Fig. 8**, clearly shows that this method can improve the high-frequency characteristics of FETs on GaAs-Si wafers.

Another possible method consists of etching and grooving the epitaxial layers, including the interfacial layer, around the gate pads to the Si substrate, thereby separating the gate pads from other portions. This corresponds to the method of making R_{gp} very large in **Fig. 7**(b).

3.3 Input-output characteristics of power MESFETs on Si wafers

The above study results show that power FETs are one of the GaAs-on-Si wafer applications closest to commercialization. Because power FETs have such a large gate width as required to control high currents, the large gate width in turn increases the gate-source intrinsic capacitance and makes C_{gp}/C_{gs} in Eq. (1) smaller than unity, so that the effect of the parasitic capacitance can be ignored. Si substrates are superior to GaAs substrates in heat dissipation and thus can deliver a higher output for the same thickness. Now that high-output and low-power consumption GaAs FETs are seeing increasing use in cellular phones and their base stations, GaAs-on-Si wafers can meet the low-price requirement of the FETs.

Fig. 9 is the cross section of a SEM photograph (**Photo 1**) of FETs trial-made for cellular phone use. The gate length is L_g = 0.8 µm, the gate width is W_g = 5.6 mm, and the gate pad area is 50 × 50 μm^2 × 2. The SiO_2 layer inserted to reduce the parasitic capacitance is located below the gate connecting bus lines and the gate pads. When the gates were as large as the FETs, the C_{gp}/C_{gs} ratio was about 0.1, and the FETs exhibited good high-frequency characteristics, irrespective of whether or not grooves were pre-

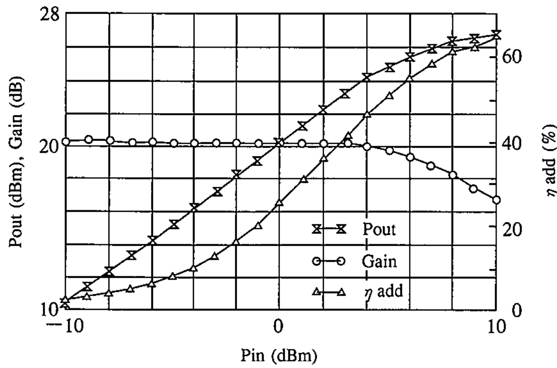


Fig. 10 Input-output characteristics of test-fabricated power MESFETs on Si wafer (W_g = 5.6 mm, measured cutoff frequency = 0.85 GHz, drain voltage V_{ds} = 3.6 V)

sent around the gates. The FETs were fabricated into a chip, packaged, and evaluated for input-output characteristics at 0.85 GHz by the load pull method. The results are shown in **Fig. 10**[17]. The gain is more than 20 dB, linearity is excellent, and efficiency is high. The characteristics of the test-fabricated power MESFETs on Si substrates are comparable or superior to those of commercial power MESFETs on GaAs substrates and are good enough for commercial applications.

4. Conclusions

The GaAs-on-Si wafer problems described in the Introduction have been shown to be solvable through the trial fabrication and evaluation of electron devices. If GaAs-on-Si wafers provide electrical characteristics equivalent to those obtainable with GaAs wafers, heat dissipation and cost advantages will be highlighted. Commercial uses will soon follow. The reliability testing of the above-mentioned devices is under way. If their reliability is verified, the GaAs-on-Si devices will be soon used as power FETs for cellular phones and their base stations.

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