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Gettering Properties of Silicon Wafer Covered by Polysilicon

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Abstract:

As a result of the comprehensive evaluation of the gettering properties of the silicon wafer covered by polysilicon, it was found that the gettering efficiency of this wafer is high for copper with greater diffusivity but low for iron with smaller diffusivity. This low gettering efficiency for iron is common to all external gettering wafers. The mechanical strength of this silicon wafer is higher than that of sand-blasted gettering wafer and similar to that of non-gettering wafer. The density of oxygen precipitates in this wafer after heat treatment is enhanced by the polysilicon layer itself.

1. Introduction

Increasing circuit density of semiconductor devices calls for increasing cleanliness in the device fabrication process, but there still are some contaminants that are unintentionally introduced during the process. The device active region at the front surface of the silicon wafer is kept clean by forming collection sites in the bulk and at the back surface of the wafer for contaminating heavy metal elements. This procedure is called gettering.

Gettering is divided into two groups: internal gettering (IG) and external gettering (EG). Internal gettering is achieved by forming gettering sites in the bulk of the wafer, while external gettering is characterized by the formation of gettering sites at the back surface of the wafer[1]. With the internal gettering method, oxygen supersaturated in Czochralski (CZ) silicon wafer is precipitated only in the bulk of the wafer through controlled heat treatment. External gettering is subdivided, by the way defects are introduced into sandblasting, polysilicon film deposition, laser damage, ion implantation, and phosphorus diffusion.

All these gettering methods have both merits and demerits, but must meet the following requirements on the whole. High gettering efficiency must be maintained throughout high-temperature heat treatment for complementary metal oxide semiconductor (CMOS) process and other processes. As side effects, generation of contaminants and particles by the gettering treatment must be little, and so be wafer warpage. The polysilicon film deposition method is to form a polysilicon film on the back surface of the wafer. Since the gettering sites are grain boundaries, they are presumed to have high defect density and not to readily disappear through high-temperature heat treatment. This method is superior in cleanness because it utilizes pyrolytic reaction of silane used in the semiconductor device fabrication process.

The gettering properties of the wafer with polysilicon film coated by the method, which is obviously best suited under the above-mentioned conditions, are compared with those of the sandblasting method and the internal gettering method having high gettering efficiency.

2. Fabrication of Polysilicon Film-Coated Gettering Wafers and Evaluation of Crystallinity

The polysilicon film was formed by utilizing the pyrolytic reaction of silane in the low-pressure CVD process, a typical polysilicon film formation technique. Usually, polysilicon is deposited over the temperature range of 600°C to 700°C. The crystallinity of polysilicon grains is known to change with the deposition temperature[2].

The change in the crystallinity of the polysilicon film with the deposition temperature and the change in the structure of the polysilicon film with the CMOS heat treatment simulation were

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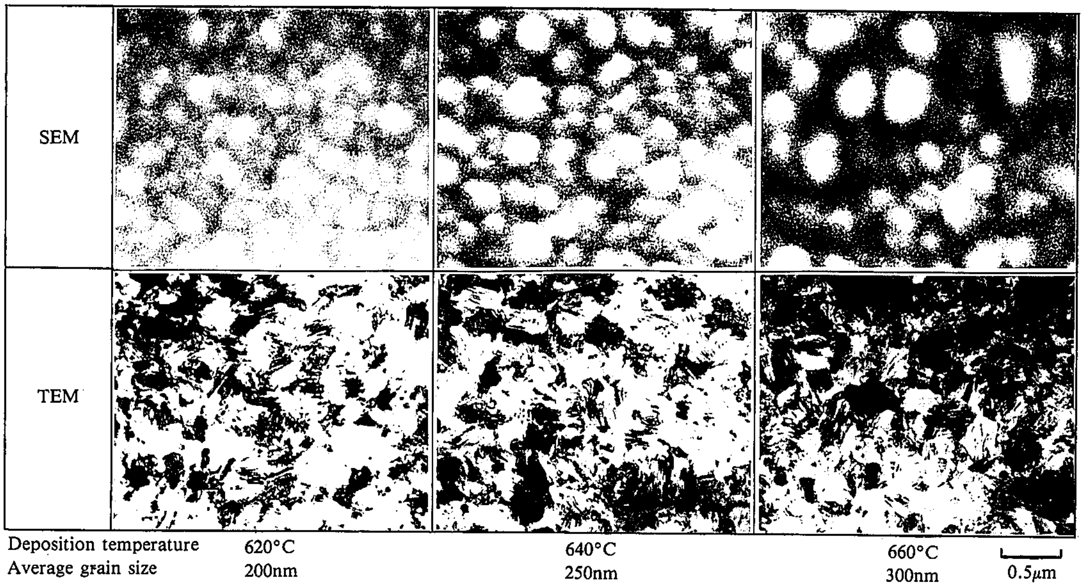


Photo 1 Effect of polysilicon film deposition temperature on grain size

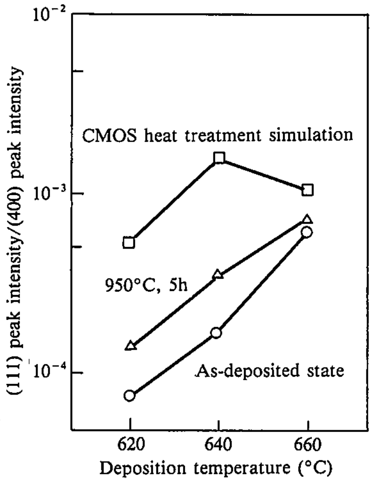
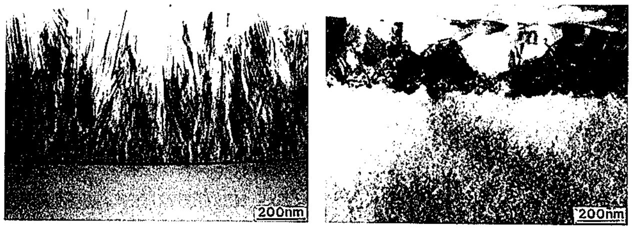


Fig. 1 Polysilicon film deposition temperature and (111) plane diffraction intensity, and their changes with heat treatments



(a) As deposited state (b) CMOS heat treatment simulation

Photo 2 Cross-sectional TEM micrographs of polysilicon films

evaluated by scanning electron microscopy (SEM), transmission electron microscopy (TEM), and X-ray diffraction technique.

Photo 1 shows the change in the grain size of the polysilicon film with the deposition temperature. The grain size of the polysilicon film increases with increasing deposition temperature. **Fig. 1** shows the results of polysilicon film crystallinity as evaluated by the X-ray diffraction technique. The change in the (111) peak diffraction intensity with the deposition temperature is evident. Heat treatment at 950°C for 5 h or CMOS heat treatment increases the (111) diffraction intensity and eliminates the difference in the crystallinity of the polysilicon film with the deposition temperature.

Photo 2(a) shows a cross-sectional TEM micrograph of the polysilicon film. A columnar grain structure is observed in the as-deposited state. The grain structure of the polysilicon film observed after the CMOS heat treatment is shown in **Photo 2(b)**[3]. The CMOS heat treatments were conducted under representative conditions of annealing in wet oxidation at 1,000°C for 3 h, annealing in nitrogen at 1,200°C for 7 h, annealing in nitrogen at 800°C for 2 h, and annealing in wet oxidation at 1,000°C for 4 h. It is clear from the figure that the heat treatment in the oxidizing atmosphere oxidizes the polysilicon film and reduces its thickness. The heat-treated polysilicon film is free from columnar grains which are observed in the as-deposited state, and exhibits coarsened grains and twins. Solid-phase epitaxial growth is evident on the polysilicon film side of the polysilicon film/substrate interface.

It should be noted that the quality of the polysilicon film more greatly changes with the progress of heat treatment than with the deposition temperature. This change in the quality of polysilicon film is thought to influence the gettering efficiency.

3. Gettering Properties

The gettering efficiency of polysilicon film-coated wafers was evaluated by intentionally contaminating them with copper and iron, representative contaminating metals. The wafers were contaminated by the spin coating method with a solution containing heavy metals, and the amount of deposited contaminants was evaluated by atomic absorption spectrophotometry (AAS).

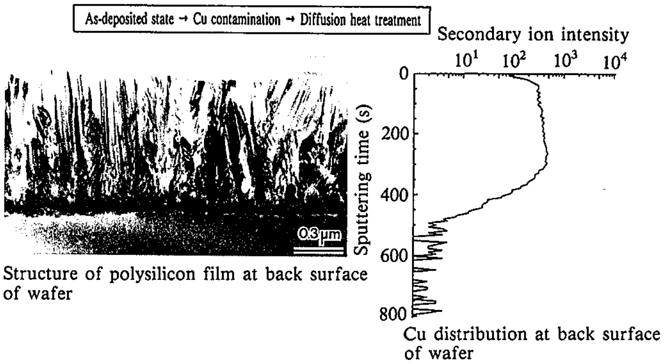
3.1 Gettering effect on copper impurity

The copper gettering efficiency of polysilicon film-coated wafers and gettering sites therein were evaluated by secondary ion mass spectroscopy (SIMS) and by AAS from the amount of initial contaminants collected from the gettering sites. Copper can fully diffuse in the wafer through annealing at 1,000°C for 30 min.

The copper distribution in the polysilicon film at the back surface of the wafer as examined by SIMS is as shown in **Fig. 2**. It is clear from the figure that the polysilicon film itself constitutes the main gettering site for the copper impurity. The amount of copper collected from the film as determined by AAS is as shown in **Fig. 3**. Of the initial amount of contaminating copper, 75% to 85% is gettered in the polysilicon film.

The gettering efficiency was then evaluated by measuring the generation lifetime with high sensitivity[4]. The wafers were of the n-type fabricated by the magnetic field-applied Czochralski (MCZ) method, and had a resistivity of 10 Ω·cm with oxygen concentration of 3×10^{17} atoms/cm^3. MCZ wafers having lower oxygen concentration than that of conventional CZ wafers were used to eliminate the internal gettering effect during the heat treatment process. Non-gettered wafers and back-surface sandblasted wafers were similarly evaluated for comparison. The generation lifetime was determined by fabricating MOS diodes on the wafer surface and measuring the MOS capacitance-time relationship.

The gate oxidation of the MOS diodes was conducted in a dry oxygen atmosphere at 1,000°C for 25 min. The diffusion of copper from the surface into the bulk of the wafer was accomplished in this step. The thickness of the oxide film formed was 280 Å. The initial amount of surface contamination was 7×10^{13} atoms/cm^2. **Fig. 4** shows the change of generation lifetime with heat treatment. The open marks indicate contaminated wafers, while the solid marks indicate non-contaminated. When the wafers are not gettered, the copper contamination reduces the generation lifetime by four orders of magnitude. The generation lifetime is not shortened when the polysilicon film-coated wafers are not annealed before contamination or are annealed in a single step in a wet oxygen atmosphere at 1,100°C for 1 h, but is cut by about one order of magnitude after the CMOS heat treatment. The generation lifetime is cut by about two orders of magnitude when the sandblasted wafers are not annealed before contamination or are annealed in a single step in a wet oxygen atmosphere at 1,100°C for 1 h, but is cut by about three orders of magnitude after the CMOS heat treatment.



Structure of polysilicon film at back surface of wafer

Cu distribution at back surface of wafer

Fig. 2 Cross-sectional TEM micrograph of copper-contaminated polysilicon film-coated wafer and copper distribution by SIMS

As can be seen from **Photo 2(b)**, the structure of the polysilicon film after the CMOS heat treatment changes from boundaries with small angular deviation due to columnar grains in the as-deposited state to boundaries with large angular deviation due to grain coarsening. This change leads to an increase in the gettering efficiency of gettering sites themselves. Solid-phase epitaxial growth from the substrate/polysilicon film interface into the polysilicon film and the reduction in the polysilicon film thickness due to annealing and the oxidation treatment lead to a decrease of gettering sites, which in turn reduces the gettering efficiency. The gettering efficiency of polysilicon film-coated and heat-treated wafers, therefore, depends on the balance of these contradictory merits. The decrease in the gettering efficiency of polysilicon film-coated wafers after the CMOS heat treatment may be mainly explained by the decrease of gettering sites.

Photo 3 shows the surface defects observed by surface wright etching. It is known from the photo that the surface defects

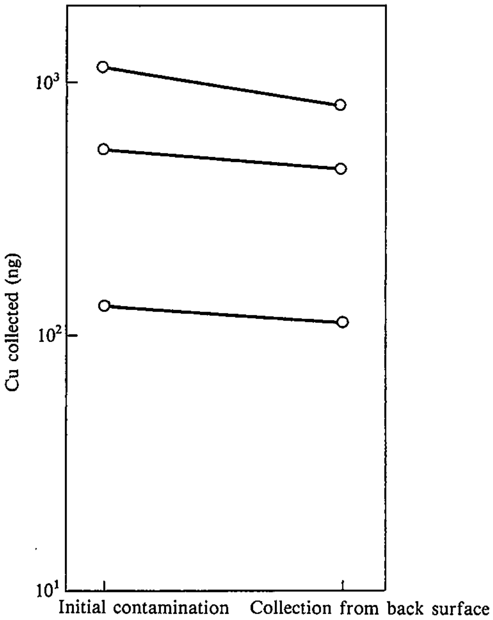


Fig. 3 Initial copper contamination and back-surface copper collection in copper-contaminated polysilicon film-coated wafers as examined by atomic absorption spectrophotometry

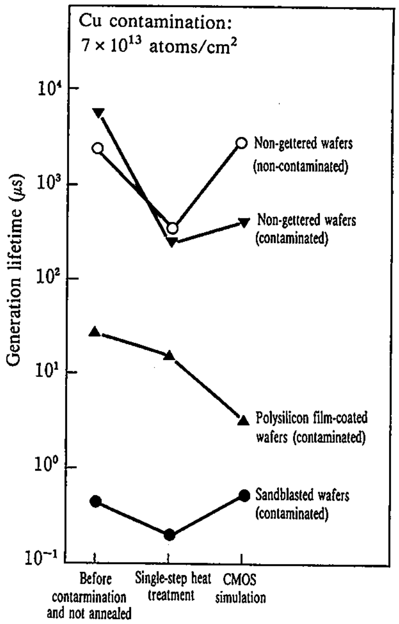


Fig. 4 Change in generation lifetime depending on heat treatment of copper-contaminated wafers

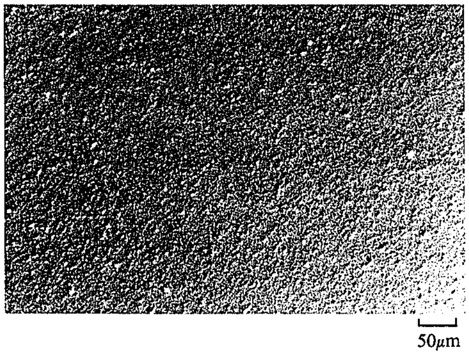


Photo 3 Surface defects in copper-contaminated wafer by wright etching

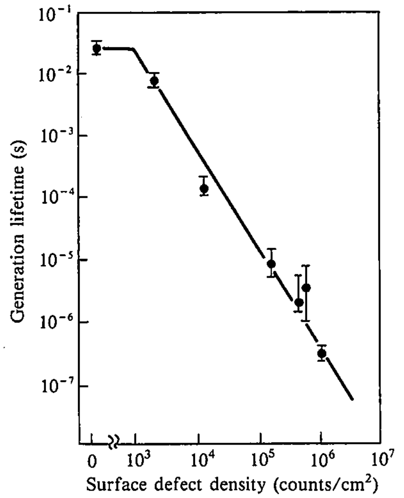


Fig. 5 Surface crystal defects versus generation lifetime

originate in copper. **Fig. 5** shows the correlation between the defect density and the generation lifetime. The generation lifetime decreases with increasing defect density. The decline of generation lifetime may be ascribed to the formation of silicide due to copper contamination or the occurrence of dislocations as a secondary defect.

Polysilicon film-coated wafers thus have a high copper gettering efficiency. Optimization of the film thickness considering the CMOS heat treatment, for example, is expected to provide a still higher gettering efficiency.

3.2 Gettering effect on iron impurity

As on copper impurity, the gettering effect on iron impurity was evaluated with AAS from the generation lifetime and the amount collected.

The wafers used were p-type CZ wafers with resistivity of 10 Ω·cm. The back-surface polysilicon film thickness of polysilicon film-coated wafers was 1.0 µm, and the oxygen concentration was 7.5×10^{17} atoms/cm^3. The initial oxygen concentration of internal-gettered wafers was 9.5×10^{17} atoms/cm^3. The internal gettering process comprises three steps, annealing at 1,100°C for 10 h, annealing at 650°C for 16 h, and annealing at 1,000°C for 10 h. The denuded zone (DZ) width was 40 µm.

In the MOS diode fabrication process, the gate oxidation process was parformed continuously in a dry oxygen ambient at 1,000°C for 25 min after iron diffusion in a nitrogen atmosphere at 1,000°C for 1 h, because iron is slower to diffuse than copper and is readily incorporated in the oxide film.

Fig. 6 shows the change of generation lifetime with increasing surface iron contamination. Internal-gettered wafers exhibit a gettering effect, while polysilicon film-coated wafers and sandblasted wafers do not.

To clarify the gettering effect of polysilicon film-coated wafers respectively on copper and iron, the gettering efficiency was evaluated through slow cooling treatment. Wafers were slow-cooled under the following three different cooling conditions after oxidation at 1,000°C. The first condition was that the wafers were removed from the furnace at 1,000°C after the oxidation; the second: cooled from 1,000°C to 800°C at 3°C/min and removed from the furnace at 800°C; and the third: cooled from 1,000°C to 800°C at 0.1°C/min and removed from the furnace at 800°C. The wafers shown in **Fig. 6** were evaluated under the second condition. **Fig. 7** shows the cooling condition dependence of the amount of iron collected from the back-surface polysilicon film relative to the amount of initial iron contamination. As indicated, the iron collection from the polysilicon film is not large when the wafers are removed as oxidized at 1,000°C or after cooling to 800°C at the rate of 3°C/min, but is large enough to demonstrate a gettering effect when cooled at the rate of 0.1°C/min and removed at 800°C. **Fig. 8** shows the effect of slow cooling on the generation lifetime of iron-contaminated wafers. The polysilicon film-coated wafers also exhibit the gettering effect.

The effect of cooling conditions on the gettering efficiency of polysilicon film-coated wafers is arranged hereunder from the

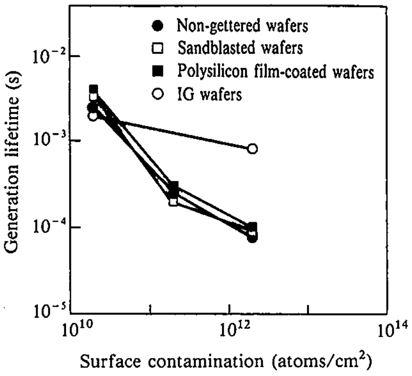


Fig. 6 Change in generation lifetime of iron-contaminated wafers

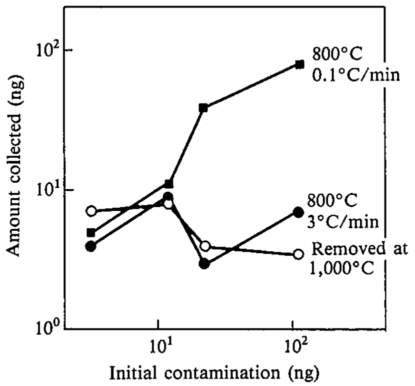


Fig. 7 Cooling rate dependence of iron impurity collection from back-surface of polysilicon film-coated wafers in relation to initial iron contamination

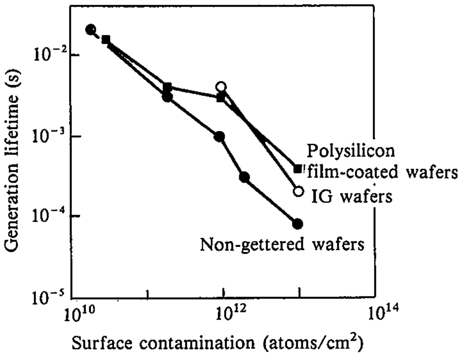


Fig. 8 Change in generation lifetime of iron-contaminated wafers with slow cooling conditions

viewpoint of diffusion distance from the supersaturated state. A contamination amount of 100 ng/wafer translates into 1.4×10^{14} atoms/cm^3 if the contaminant is uniformly diffused into the bulk of the wafer. This is equivalent to a solubility at 950°C[5]. The total diffusion length of iron is 640 μm at 3.0°C/min and 3.5 mm at 0.1°C/min, respectively, during cooling from 950 to 800°C. Some degree of supersaturation is considered necessary for precipitation to occur, and the diffusion distance is thought to be much smaller than the calculated values mentioned above. The wafer thickness is about 650 μm, and therefore, gettering is not enough at the cooling rate of 3°C/min, probably because the diffusion distance from the supersaturated state is not as large as the wafer thickness. Since the distance to gettering sites is 40 μm, internal-gettered wafers can be fully gettered.

When external-gettered wafers, including polysilicon film-coated wafers, are cooled at the normal rate of 3°C/min, gettering from the supersaturated state cannot be expected because of the diffusion limit process.

4. Effect of Polysilicon Film in Inducing Oxygen Precipitation

An annealing temperature in the vicinity of 650°C is known to induce the nucleation of oxygen precipitation in conventional CZ silicon wafers. The polysilicon film deposit is annealed at 650°C for about 2 h. The oxygen precipitation is thus considered to increase in polysilicon film-coated wafers. The effect of the polysilicon film itself in precipitating oxygen is also pointed out[6,7]. To confirm this phenomenon, the effect of polysilicon film deposition on oxygen precipitation was evaluated as to the change of oxygen concentration in the substrate.

Wafers coated with a polysilicon film and wafers annealed in the same way as done for the polysilicon film deposition were treated to precipitate oxygen (annealed at 900°C for 4 h and at 1,000°C for 16 h). The relationship thus established between the initial oxygen concentration (O_i) and the oxygen precipitation (ΔO_i) is as shown in **Fig. 9**, wherein the oxygen precipitation is the difference between the initial oxygen concentration and the oxygen concentration after annealing. The solid line indicates the amount of oxygen precipitation when annealing is not made of the polysilicon film deposition. Oxygen precipitation is promoted by annealing the polysilicon film deposition and is accelerated further by the polysilicon film itself.

Fig. 10 shows the oxygen precipitate density distribution in the wafer cross section. The defect density of polysilicon film-coated wafers does not depend on the initial oxygen concentration. The precipitate density in the back surface of the wafer or polysilicon film-deposited surface is higher than that in the front surface and bulk of the wafer. When the wafer is annealed for the polysilicon film deposition, its defect density distributions in the front-surface and bulk are the same as in polysilicon film-coated wafers. The increase in the amount of oxygen precipitation in the polysilicon film may be explained by a difference in the defect density of the back surface. The polysilicon film itself has an effect of inducing the oxygen precipitation. Its possible mechanism is that the polysilicon film provides site for the generation and termination of point defects (vacancy and interstitial silicon) to promote the oxygen precipitate formation reaction[6,7].

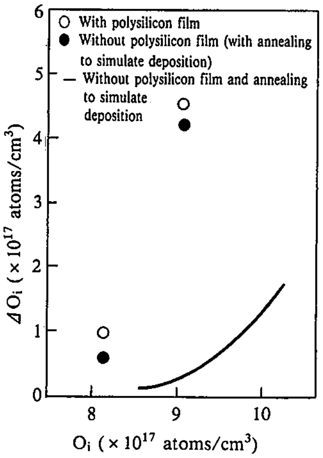


Fig. 9 Oxygen precipitation behavior of polysilicon film-coated wafers

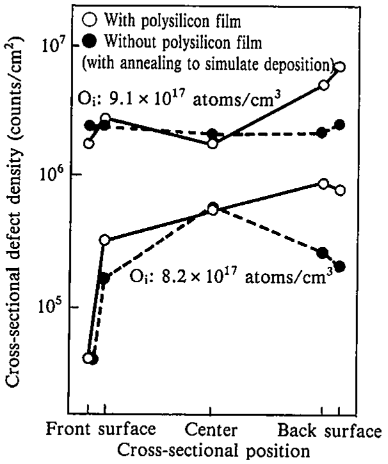


Fig. 10 Cross-sectional defect distribution in polysilicon film-coated wafers after oxygen precipitation annealing

In this way, polysilicon film-coated wafers can receive gettering by grain boundaries and combined gettering by oxygen precipitation.

5. Warpage Behavior

A harmful effect of gettering is warpage. Wafer warpage causes improper focusing during lithography and allows dislocations to pass through the active region of devices, resulting in a device failure. To obtain a high gettering efficiency, however, it is desirable to obtain a high crystal defect density, which in turn promotes the wafer warpage. An optimum gettering treatment is therefore called for.

The warpage of a polysilicon film-coated wafer before polysilicon film deposition is less than 10 μm in thickness. When the front surface is mirror polished and the polysilicon film is left on the back surface only, the mirror-polished front surface warps in a concave form. The concave warpage is about 40 μm when the film deposited on the back surface is 1 μm thick. Annealing the polysilicon film-coated wafer at 1,000°C for about 1 h can restore the warpage to its original state before the polysilicon film deposition. This means that the elastic stresses developed by the back-surface polysilicon film in the polysilicon film-coated wafers can be easily removed by annealing.

The strength at elevated temperatures of wafers was then evaluated by forced warpage[8]. High thermal stresses were imposed on the wafers by inserting and withdrawing them at higher-than-normal speeds. Sandblasted wafers were similarly evaluated for the sake of comparison. At 1,100°C, the wafers were inserted and withdrawn at speeds of 150, 300, 600, and 900 mm/min. **Table 1** shows the resultant warpage of wafers under these conditions. The sandblasted wafers exhibit sharply increasing warpage with increasing speed, while the non-gettered wafers and the polysilicon film-coated wafers do not increase in warpage with increasing speed. This indicates that non-gettered wafers and polysilicon film-coated wafers have satisfactory high-temperature mechanical strength.

As described above, the polysilicon film-coated wafers were found to suffer a minimum degree of warpage as a side effect.

6. Conclusions

It may be concluded from the above discussion that polysilicon deposition is an excellent gettering method on the whole. One problem is low gettering efficiency against iron contamination. The most probable limiting factor is the diffusion distance of iron impurity relative to the gettering site, which is a problem common to external gettering methods. Recently, gettering for iron by phosphorus diffusion has been reported[9]. Utilization of such a new gettering technique is indispensable for developing further advanced polysilicon film-coated wafers.

Table 1 Change in warpage with inserting and withdrawing speed (preliminary annealing in wet oxidation ambient at 1,100°C for 1 h)

(μm)

Speed (mm/min)	150	300	600	900
Non-gettered wafers	2	2	1	2
Sandblasted wafers	22	40	79	82
Polysilicon film-coated wafers	1	2	1	2

References

1) Science Forum: ULSI Process Data, p. 267
2) Sze: VLSI Technology. p. 102
3) Saga, M. et al.: Extended Abstracts of 50th Annual Meeting, 1989, Japan Society of Applied Physics, p. 297
4) Ishisaka, K. et al.: Extended Abstracts of 37th Annual Meeting, 1990, Japan Society of Applied Physics, p. 224
5) Weber, E.R.: Apply. Phys. A30, 1 (1983)
6) Hahn, S. et al.: Mat. Res. Soc. Symp. Proc. 59, 353 (1986)
7) Yang, K.H., Tan, T.Y.: Mat. Res. Soc. Symp. Proc. 36, 223 (1985)
8) Tanaka H. et al.: Extended Abstracts of 37th Annual Meeting, 1990, Japan Society of Applied Physics, p. 227
9) Nadahara, S. et al.: Proc. of 16th Intern. Conf. on Defects in Semiconductors, p. 667