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Development of Molded TAB Package Technology

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Abstract:

Molded TAB (Tape Automated Bonding) package technology was developed for multi-pin and fine-pitch LSI packages to be used in electronic equipment of higher functionality, and smaller size and weight. The transferred bump TAB process was studied as the method of inner lead bonding for multi-pin and fine-pitch electrodes from the LSI chip, and transferred bump TAB conditions to a pitch of 138 μm were clarified. Transfer molding, a high-reliability plastic encapsulation process, was investigated for application to TAB, and transfer molding conditions to a package thickness of 1.80 mm were clarified. Packages fabricated as samples by applying the transferred bump TAB method and transfer molding method performed well in terms of both functionality and reliability.

1. Introduction

Recent years have seen dramatic reductions in the size, weight, and thickness of electronic equipment with rapidly increasing functionality of semiconductor products. Take the civilian electronic equipment field as an example. Personal computers evolved from the laptop type to the notebook type, and a still smaller palmtop type has been announced. Cellular phones and camcorders have improved in functionality while decreasing in size, adding to their commercial attractiveness. Even such a high-functionality product as a combination of camcorder, cellular phone and personal computer will be introduced in the near future.

High-performance, multi-functional and small-sized electronic equipment require an increase in the density of LSI circuits and eventually the consolidation of multiple chips into a single chip. This demand has accelerated the trends toward a higher pin count, operating frequency, and power consumption of LSI, which in turn has called for matching LSI packages and printed circuit board packaging methods. Formerly, packages were supposed only to perform their basic functions of protecting semiconductor devices from the environment and facilitating the handling of semiconductor devices. As semiconductor devices advanced in functionality, the functions required of packagaes diversified. Many LSI users strongly demand such functions as 1) higher pin count, 2) smaller size and thickness, 3) higher speed, 4) lower thermal resistance, and 5) multi-chip configuration, with the condition of a lower price.

Against this background, the authors started in 1990 work on the development of molded tape automated bonding (TAB) packages that feature a high pin count, small size and thickness, low cost, and high reliability.

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2. Development of molded TAB packages

2.1 Aim of molded TAB package

The quad flat package (QFP) and pin-grid array package (PGA) are common package types that provide for multiple pins and high density. Recently, the tape carrier package (TCP) using TAB tape is appearing on the market. The optimum density range of these packages is shown in **Fig. 1**[1]. The lower the pack-

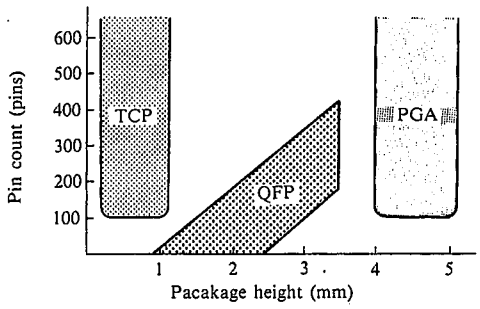


Fig. 1 Increase in circuit density of packages

Table 1 Comparative evaluation of QFP, PGA, and TCP

	QFP	PGA	TCP
Price	○		
Pin count		○	○
Size and thickness	○	○	○
Speed			○
Thermal resistance		○	

age height and the higher the pin count, the higher is the packageing density. **Table 1**[1] compares the characteristics of the QFP, PGA, and TCP. The PGA is suited for mutiple-pin, high-speed, low-thermal resistance, and high-reliability LSI chips, but is expensive. The QFP can be supplied at lower cost than the PGA and TCP, and is a predominant type of package now.

The TCP is best suited for multi-pin, small-sized, and small-thickness LSI chips, and is used in multi-pin liquid crystal drivers by vintue of this characteristic. It is not applied to common LSI circuits such as application-specific integrated circuits (ASICs), because peripheral technology is not established yet, as evident form the problems of bump forming cost, quality, seal moisture resistance, and printed circuit board packaging. As the TCP will undoubtedly become a primary type of package in the futrue, the authors tried a drastic modification to the present TCP. Key points in the modification are as follows:

(1) Bump formation
Bumps are conventionally formed on the LSI chip side. This method however, involves problems with manufacturing capacity, reliability, and cost. Therefore, apply the transferred bump TAB process[2] that forms bumps on the TAB tape side.

(2) Improvement in moisture resistance
Conventional TAB seals chips by potting, but this sealing method is not suited for ASIC applications where high reliability is demanded. Therefore, develop a new method of sealing with a high-reliability transfer molding[3] used for the QFP.

(3) Increase in speed
Reducing the wire length through a size reduction favors a speedup. In the future, the TAB tape will be wired in two layers to ensure impedance matching and reduce power supply inductance.

(4) Reduction in thermal resistance
Improve the package structure to make up for the poor thermal conductivity of resin systems.

Work was initiated on the development of molded TAB packages that would be at least acceptable in meeting the requirements listed in **Table 1**. The development work was designed to TAB pacakge two types of LSI for the main board system and controller of a notebook personal computer under development then, to establish peripheral technology for fabricating the package and mounting them on substrates, and to verify the functionality and reliability and reliability of the prototype package. This study was completed on a 180-pin, 16-mm square, and 1.8-mm thick molded TAB package in April 1991. The molded TAB pacakge are under evaluation.

2.2 Development of molded TAB package

2.2.1 Outline of molded TAB packaging process

Table 2 lists the data of LSI chips, TAB tapes, and packages under evaluation. The LSI chips are C-MOS logic LSI chips manufactured to the conventional wire bonding specification. **Fig. 2** schematically shows the molded TAB packaging process. The process consists mainly of an inner lead bonding (ILB) step where aluminum electordes, or LSI chip input and output terminals, and TAB tape leads are thermocompression bonded through gold bumps; the molding step where the LSI chip is encapsulated in plastic to protect against external environments and forces; and the comprehensive electrical testing step where the completed LSI product is tested.

The product form is such that each molded TAB pacakge is fitted into a TAB carrier (Yamaichi Denki IC35006), as shown in **Fig. 2**. Using a Sentry tester porgram obtained from VLSI Technology and converted into an Advantest tester program, and a TAB test socket (Yamaichi Denki IC51-224-1191), each prototype molded TAB pacakge was DC, AC, and function tested. The reliability of the molded TAB packages was evaluated according to applicable MIL standards. The molded TAB package

Table 2 Parts used

Item	Chip A	Chip B
(A) LSI chip		
• Chip size	8.1 ×9.0 mm	9.25 ×9.18 mm
• Electrode size	95 × 95 μm	110 × 110 μm
• Number of terminals	180	179
• Electrode pitch	138 μm	150 μm
• Power consumption	0.5 W	0.5 W
(B) TAB tape	35 mm Super	
• Inner lead width	75 μm	80 μm
• Outer lead width	100 μm	100 μm
• Outer lead pitch	280 μm	280 μm
(C) Transferred bump		
• Bump hardness	40-50 HV	
• Bump diameter	70 μm	90 μm
• Bump height	25 μm	25 μm

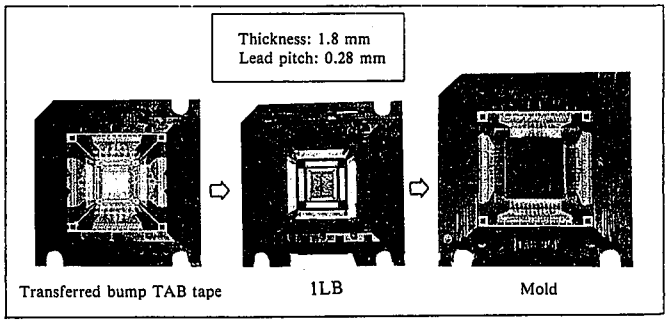


Fig. 2 Molded TAB packaging process

was loaded in each environmental test apparatus, removed after the specified length of time, subjected to overall electrical and appearance tests, for judging whether or not it met the test requirements.

The molded TAB package thus completed is mounted on a printed wiring board with all necessary electrical components but the TAB and has outer leads bonded to the board. The molded TAB pacakge footprint is precoated with 10 μm of solder (4/6). (The outer lead bonding or OLB process consists of outer lead cutting, forming, aligning, mounting, and thermocompression bolding.) **Fig. 3** shows a general view of the board on which the molded TAB package in mounted. Such a board was incorporated in a personal computer and checked for operation. It was found to operate without any problem.

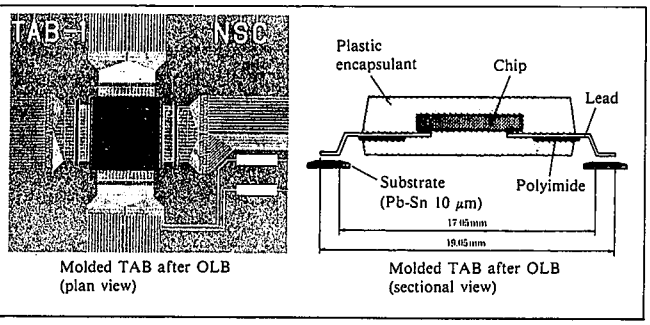


Fig. 3 OLB of modled TAB package

The TAB package is characteristic in that all electrical tests can be performed on the TAB tape and that the outer leads are cut and formed immediately before the package is mounted on the board, so that lead bends, bonding variations, and other bonding troubles are very infrequent. TAB is thus considered the best means for handling multi-pin, fine-pitch, thin, and weak leads.

2.2.2 Study of ILB transferred bump TAB process*1 for application

Traditionally, electrodes of semiconductor devices were interconnected by wire bonding. As noted above, the increasing circuit density of semiconductors in recent years has enhanced the trend toward LSI electrodes with a higher pin count and finer pin pitch. As a result, semiconductor devices can be reduced in size and cost and can be improved in reliability against thermal stress. The electrode pitch of multi-pin and narrow-pitch LSI chips is limited to 114 μm on current production basis (4.5 mm in wire length)[1] by such wire bonding problems as the geometrical constraint of the capillary (a tool for connecting a wire to a chip electrode), micromachining limit of lead frame, and length of wire.

Under these circumstances, TAB is considered another viable means of increasing the pin count and decreasing the pin pitch of LSI chips. As described earlier, howerver, TAB requires bumps. Usually, barrier metal against diffusion, such as TiW or CrCu, is formed on LSI electrodes, and gold bumps are formed by plating. These bumps are called IC bumps. This process lowers the LSI yield and requires a large amount of equipment investment. This is one reason why the use of TAB has been limited to liquid crystal drivers without diffusing into other fields of application. The transferred bump TAB process[2] was developed to solve this problem.

The transferred bump TAB process does not form bumps on the LSI chip, but forms bumps on another substrate, transfers the bumps onto the TAB tape, and bonds the bump leads to the LSI chip electrodes. This process does not require any special treatment on the LSI chip side and therefore is a very attractive process. It has the following fabrication problems, however:

(1) Transferred bump bonds are gold-aluminum bonds between gold bumps and LSI aluminum electrodes, which process if the same as conventional wire bonding process in terms of bonding metallurgy. The wire bonding process can make bonds at relatively low temperatures through the combined use of heat and ultrasonic energy. The TAB process effects bonds with thermal energy alone. It takes some ingenuity to apply thermal energy to bonds with high efficiency.
(2) The bump lead position tolerance is a poor 20 μm, because of the low mechanical accuracy of transfer in the main.

For evaluation and study as to (1) above, transferred bumps were formed with a diameter of 60 μm, height of 25 μm and pitch of 135 μm, and were investigated by gang bonding, a common method for TAB. Tool/LSI parallelism tolerance, tool temperature, bond pressure, and bond time are important gang bonding parameters.

The above study of bonding revealed that it is also necessary to prevent heat from escaping because of a temperature difference between the tool and stage, to place an insulator between the bond stage and the LSI chip for minimizing the thermal stress when the tool contacts the LSI chip, and to raise the bond stage temperature to such a degree that the LSI chip is not thermally damaged. TAB leads must be shaped in the form of gull wing as shown in **Fig. 4** to prevent them from touching LSI chip edges and causing short circuits. A SUS ring was placed around the LSI chip to obtain the desired gull wing form as well as to effect inner lead bonding (ILB). It was through these additional measures that the transferred bump TAB process became practicable.

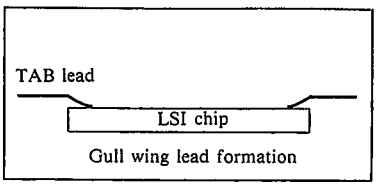


Fig. 4 Bond section after ILB

Fig. 5(a) shows the bondability window with the tool temperature and bond pressure as parameters. The bondability window of conventional IC bumps is as shown in **Fig. 5(b)**. In both cases, the difference of vertical tool inclination in relation to the IC chip was set within 3 μm, and the bumps and chip electrodes were manually alinged.

Bondability was judged according to fracture strength and mode in the sheasr test of bonds and to presence or absence of substrate damage like bond cracks in aqua regia. The open circles in **Fig. 5** indicate the conditions under which the shear sterngth is 100 g or above and no cracks are produced in underlying aluminum or silicon. It is evident from **Fig. 5** that transferred bumps provide narrower bond conditons than conventional

*1 The transferred bump TAP process is a registered trademark of Matsushita Electric Industrial Co., Ltd.

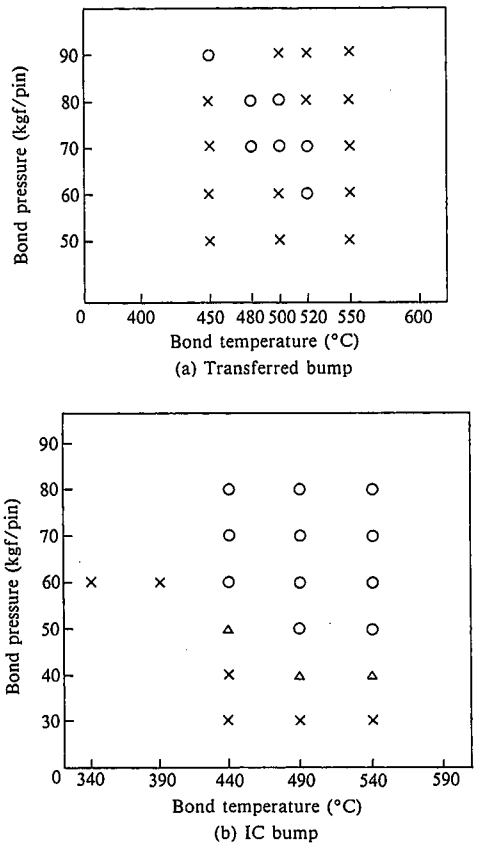


Fig. 5 Optimum temperature range

IC bumps and can be bonded only at sites where the tool temperature and load are both high, and that the tool temperature, parallelism, bump and LSI electrode positions, and other parameters must be controlled to closer tolerances for the application of the transferred bump TAB process on a production basis.

About 400 reliability evaluation samples were fabricated with a yield of 99.1% for the above-mentioned two types of LSI chips under the bonding conditions presented. A 100-μm pitch was aimed at to facilitate the application of multi-pin and close-pitched transferred bump TAP packages.

(1) Improvement in the tolerance of alignment between TAB leads and bumps from 20 to 5 μm
(2) Reduction in size of transferred bumps from 70 to 50 μm
(3) Improvement in LIB alginment tolerance
(4) Improvement in tool parallelism tolerance

The first two items will be studied by a tapemaker, while the last two items will be dealt with in house by introducing automatic production machines.

2.2.3 Development of transfer molding technology

Potting is the common method of plastic encapsulation for TAB. With the potting method, the plastic cure time is long, dripping and swelling tend to occur before complete curing, and the pacakage is susceptible to cracking. These problems make the potting process unsuitable for the plastic encapsulation of ASIC packagates that requires particularly high reliability.

The transfer molding method, which is most popluar for the plastic encapsulation of ASIC packages (pacakges with lead frames), has been studied for application to TAB. This study is led by Mitsubishi Electric Corporation. Recently, Texas Instruments of Japan has announced transfer molded TAB products. The transfer molding process consists of heating two mold halves to high temperatures, holding a lead frame bearing LSI chips between the two mold halves, melting a perform of molding compound in the pot, and forcing the melted compound into the mold cavity. This plastic encapsulation technique provide close dimensional tolerances and is suited to mass production. It had the following problems, however, when applied to the TAB tape:

(1) The TAB tape itself is thin and low in rigidity. When the molding compound is forced into the mold cavity, the TAB tape and leads are bent, and the LSI chip moves up and down in the pacakge. The latter phenomenon is called LSI chip movement.
(2) The fine pitch of outer leads (leads to be soldered to the printed wiring board) precludes the use of the conventional method of providing the lead frame with tie bars to prevent the plastic encapsulant from bleeding through the leads and pouching out the lead frame together with the tie bars after the plastic encapsulation. Removal of this plastic flash remains a problem.

A solution to the above-mentioned problem of LSI chip movement is discussed here under. This problem is much affected by mold cavity shape (such as gate shape), molding compound characteristics, and molding conditions (mold clamping pressure, transfer pressure, transfer speed, mold temperature). **Fig. 3** shows the model of LSI chip movement in a mold cavity during transfer molding. This phenomenon arises from unbalance between the top and bottom encapsulant transfer speeeds of the LSI chip and TAB tape. Given the stress imposed on the chip, the chip center should be located at the pacakage center. If this requirement is met, the encapsulant flow resistance is higher on the side B in **Fig. 6**. The mold gate shape must be designed so as to make the top and bottom gate ratio (A/B ratio in **Fig. 6**) optimum for the flow resistance of the encapsulant. It is also important that the plastic encapsulant and molding conditions be optimized so that the viscosity of the encapsulant becomes the lowest when the encapsulant flows into the mold cavity.

In the study under discussion, the encapsulant used had the lowest viscosity among commercially avaiable molding compounds. The top and bottom mold gates were fabricated as shown in **Fig. 7**, and investigation was made into the effects of the top and bottom gates and the transfer speeds on the LSI chip movement. **Fig. 7** correlates the LSI chip movement with different gate sizes as revealed in the investigation.

Fig. 8 shows the effect of transfer speed on the LSI chip movement after the gate shape optimization. As originally expected, it is evident from **Fig. 7** that the gate on the side where the encapsulant flow resistance is higher should be made larger than that on the opposite side. From **Fig. 8**, it is seen that the LSI chip position can be controlled to some degree by adjusting the transfer speed. In other words, the difference in flow resistance between the top and bottom halves can be reduced by increasing the transfer speed.

As described above, 16-mm square package molds and transfer molding conditions were studied, and conditions for prototype and short-run production were clarified.

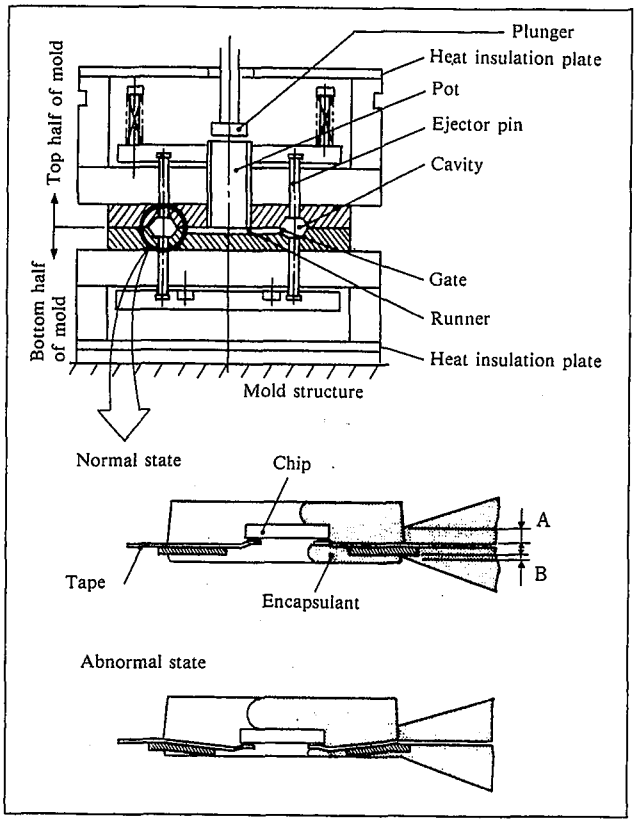
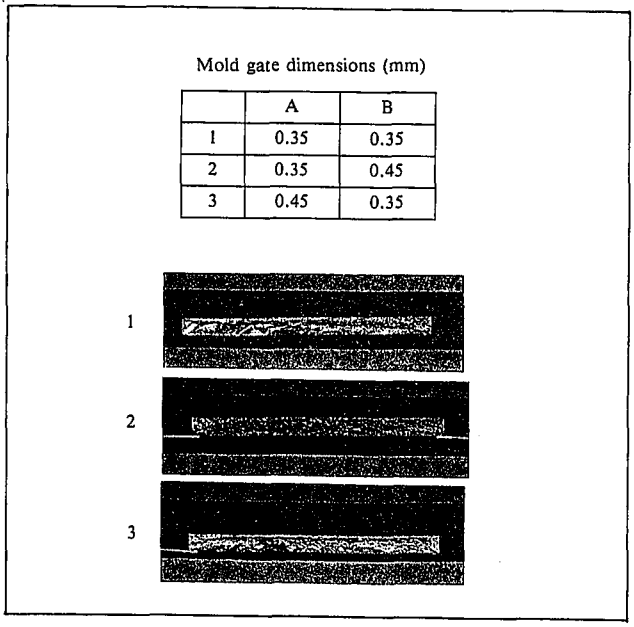


Fig. 6 Model of LSI chip movement in mold cavity during transfer molding



	A	B
1	0.35	0.35
2	0.35	0.45
3	0.45	0.35

Fig. 7 Effect of gate geomery and size on LSI chip movement in mold cavity during transfer molding

The various package needs now outstanding in respect to the thin, large, and high-heat dissipation types, will be met by implementing the following research and development projects:

(1) Standaridze the mold design by more accurately analysing the plastic encapsulant flow in the mold.

(2) Develop a plastic encapsulants of lower viscosity.

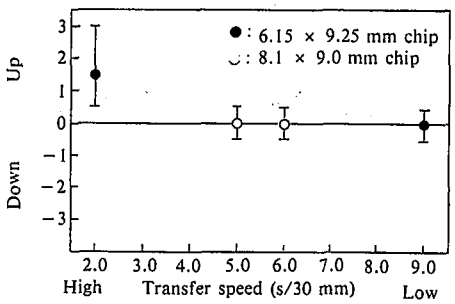


Fig. 8 Effect of transfer speed on LSI chip movement in mold cavity during transfer molding

Table 3 Results of reliability test

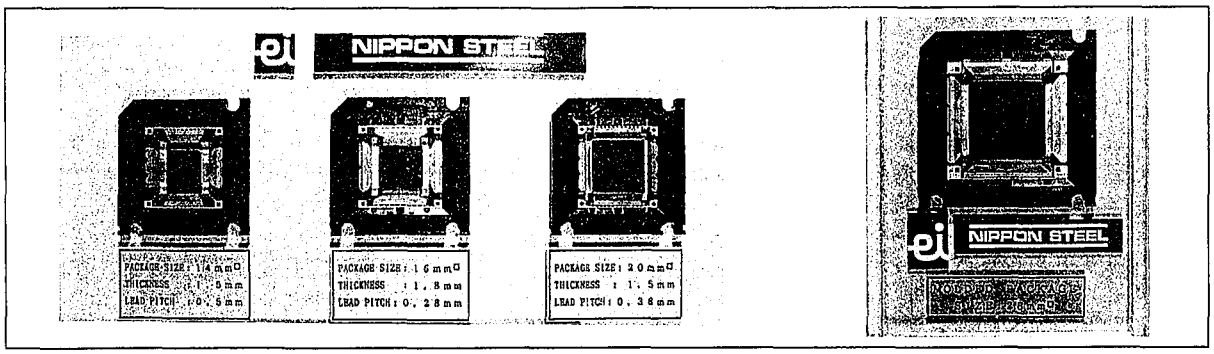
Item	Evaluation result (time-cycle) Rejects/quantity produced			
	50	200	500	1000
PCT (125°C, 2 atm)	0/83	0/83	0/83	0/83
High-temperature, high-humidity test (85°C/85%)	0/48	0/48	0/48	0/48
High-temperature, high-humidity bias test (85°C/85%, 5.5 V)	0/12	0/12	0/12	0/12
High-temperature bias test (125°C, 5.5 V)	0/11	0/11	0/11	0/11
High-temperature storage life (150°C)	0/40	0/40	0/40	0/40
Temperature cycling (30 min, −55°C/30 min, 150°C)	0/40	0/40	0/40	0/40
Thermal shock test (liquid phase, −55°C/liquid phase, 150°C)	0/40	0/40	0/40	0/40
Soldering heat resistance test ~ PCT	0/6	0/6 (PCT 96 h)	0/6 (PCT 192 h)	—
Mechanical shock test, 10 G, three directions	0/6	—	—	—

(3) Develop and commercialize an automatic production molding equipment.

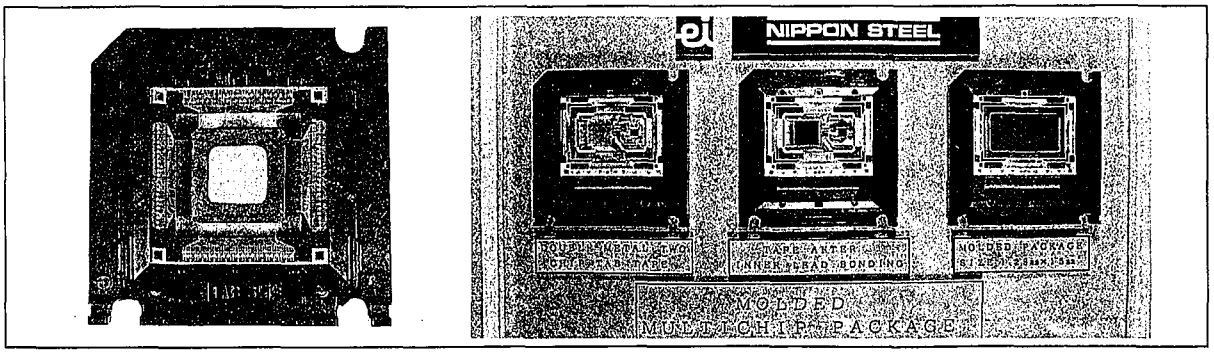
2.2.4 Overall reliability evaluation of packages

Molded TAB packages realized by implementing the above-mentioned development measures were subjected to a variety of environmental tests. The test results are as given in **Table 3**. It was confirmed in various tests that molded TAB packages are as reliable as the QFP as originally intended. The tests includes the pressure cooker test (PCT), high-temperature, high-humidity test and high-temperature, high-humidity bias test to verify the moisture resistance of the package; and the thermal cycling test, thermal shock test, and soldering heat resistance test to evaluate the structural integrity of the package.

Photo 1 shows the prototype molded TAB packages. **Photo 1(a)** is a 35-mm tape product series, and **Photo 1(b)** a 48-mm tape prodcut series. **Photo 1(c)** is a type of TAB package with heat dissipation improved by providing an aluminum plate at the back of the LSI chip. **Photo 1(d)** is a two-chip package with a two-layer wiring TAB tape.



(a) 35-mm tape (b) 48-mm tape



(c) Heat dissipation-type molded TAB (d) Multichip molded TAB

Photo 1 Molded TAB packages developed

3. Future Problems

With attention focused on the multi-pin region of 306 pins or over where the characteristics of molded TAB packages can be best exploited, the following issues will be addresed to in our future studies:

(1) Reduce the transferred bump diameter and improve the transferred bump/lead alignment tolerance.
(2) Introduce and commercialize automatic ILB equipment with improved ILB alignment and parallelism tolerance.
(3) Standardize the mold design by more accurate analysis of plastic encapsulant flow in the mold.
(4) Develop and commercialize automatic production transfer molding equipment.

4. Conclusions

In the development of molded TAB packages for electronic equipment of higher functionality, faster speed, and smaller size:

(1) Bonding conditions and problems in the application of ILB transferred bumps were clarified.
(2) Transfer molding conditions and problems in the application of transfer molding to TAB tape were clarified.
(3) Prototype molded TAB packages were proved to have good performance and reliability.

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